AN0034
Application Note

ESD protection design guide for AT32 USB interface

Introduction

This application note provides ESD protection design guide for AT32 USB 2.0 interface.

Applicable products:

MCU	AT32F403xx
	AT32F413xx
	AT32F415xx
	AT32F403Axx
	AT32F407xx
	AT32F435xx
	AT32F437xx
	AT32F425xx

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1 Overview

The hot-pluggable characteristics of the USB interface is susceptible to electrostatic discharge that damages the components, such as, crash, board burning, and disconnection and so on. It is necessary to design ESD protection on the USB interface following the two standards of JS-001-2017 (HBM) and IEC61000-4-2. HBM requires that the USB interface is capable of withstanding up to 2 kV discharge. *Figure 1* and *Table 1* shows JS-001-2017 standard test waveform and classification, and *Figure 2* and *Table 2* shows IEC61000-4-2 standard test waveform and classification.

Figure 1. JS-001-2017 standard test waveform

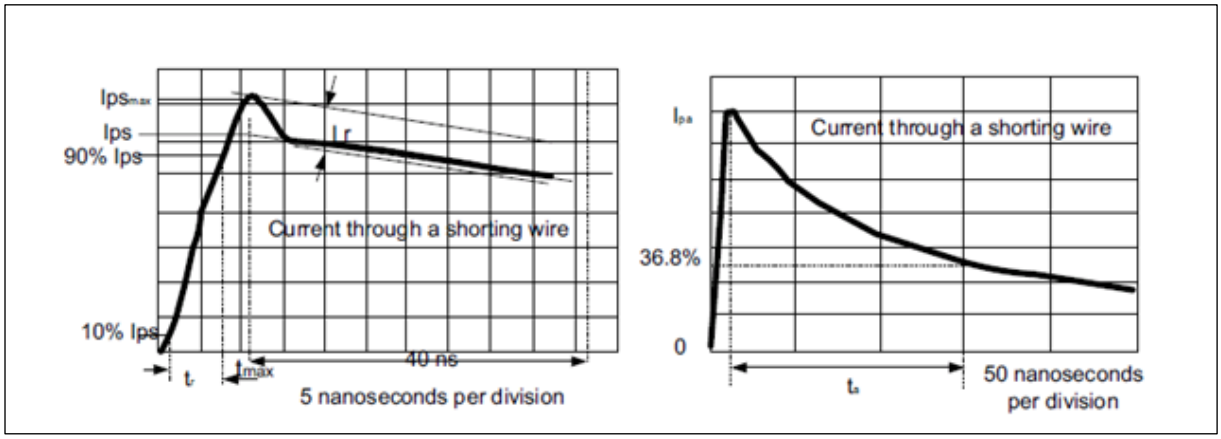


Table 1. JS-001-2017 standard class level

Class	Voltage range	Current range
Class 0	V < 250 V	I < 0.17 A
Class 1A	250 V < V < 500 V	0.17A < I< 0.33 A
Class 1B	500 V < V < 1000 V	0.33 A < I < 0.67 A
Class 1C	1 kV < V < 2 kV	0.67 A < I < 1.33 A
Class 2	2 kV < V < 4 kV	1.33 A < I < 2.67 A
Class 3A	1 kV < V < 8 kV	2.67 A < I < 5.33 A
Class 3B	V > 8kV	I > 5.33 A

Figure 2. IEC61000-4-2 standard test waveform

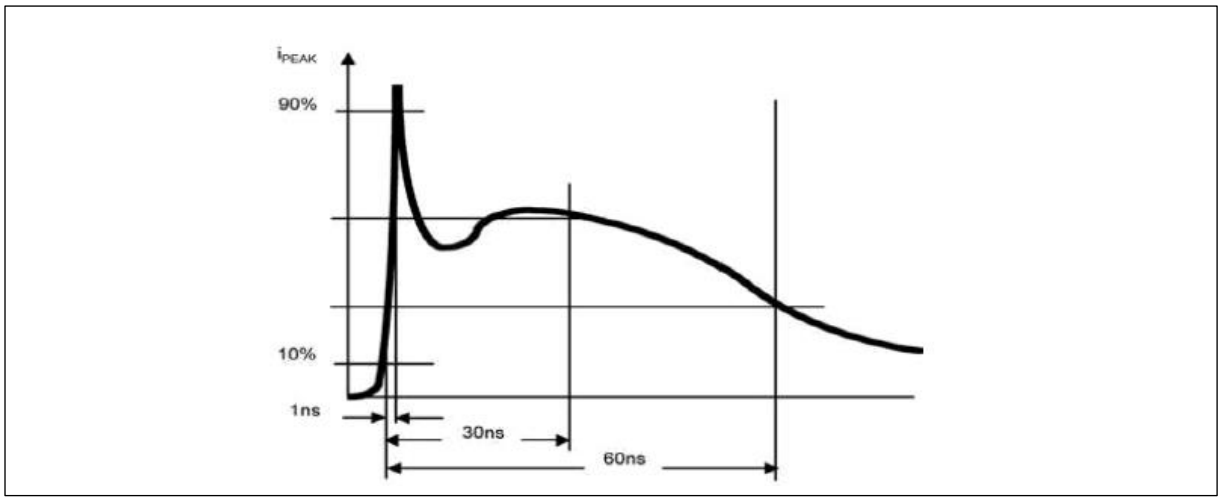


Table 2. IEC61000-4-2 standard class level

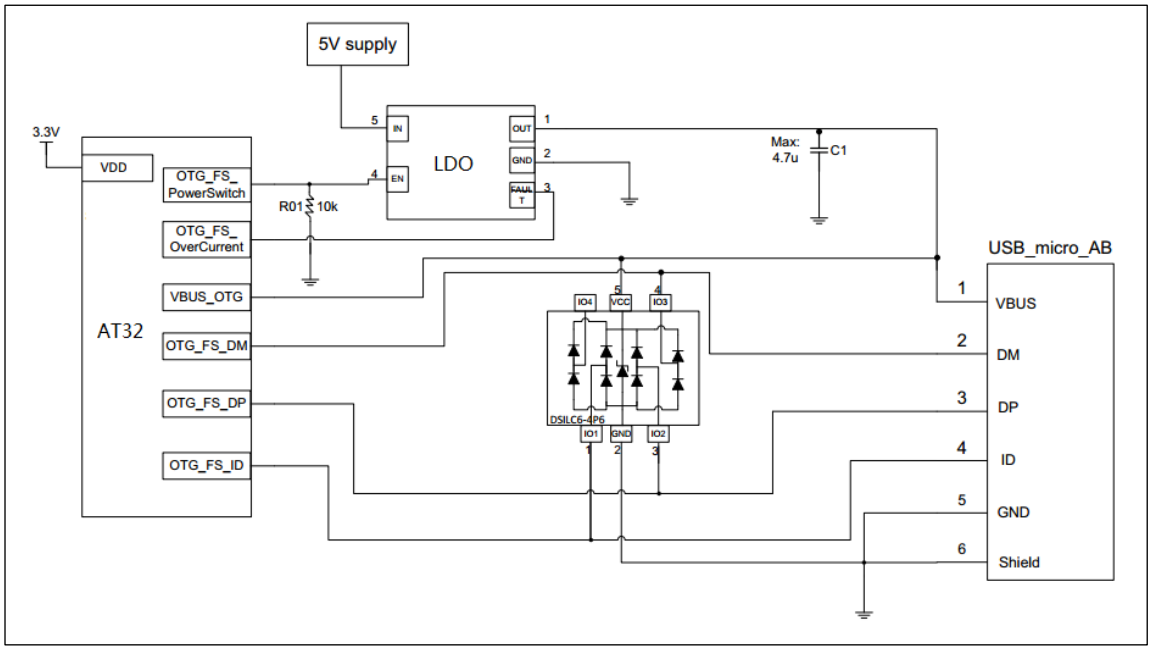
Level	Contact	Air	Peak current (A)
	indicated voltage (kV)		
1	2	3	7.5
2	4	4	15
3	6	8	22.5
4	8	15	30

2 ESD protection design tips

It is recommended to add ESD protection device and VBUS monitoring circuit to detect overvoltage when designing USB interface. Design tips are as follows:

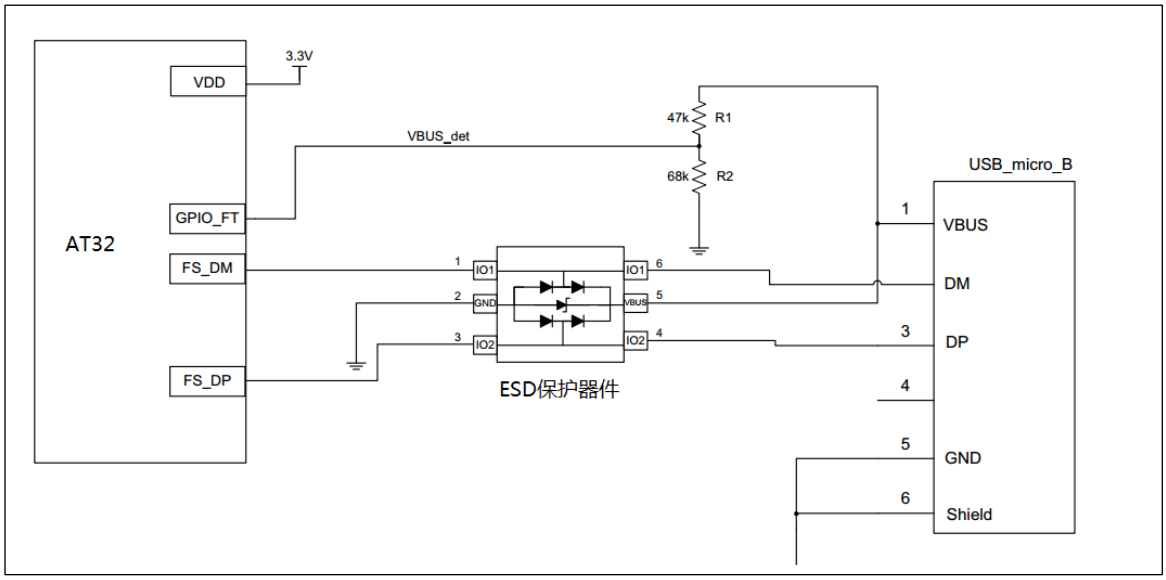
- ESD protection device should be placed close to the USB socket interface (ESD entry point) as much as possible
- VBUS, USB data line (USB_D+/USB_D-) and ID (if OTG) must be protected against ESD.

Figure 3. USB ESD protection circuit



- VBUS track should be isolated from D+/D- as much as possible
- The metal housing of USB socket must be connected to the device housing ground
- When the VBUS supply is not neededed, it can be connected to non-5V-tolerant I/O through a resistor voltage divider, or to 5V-tolerant GPIO directly, used as VBUS detection signal.

Figure 4. VBUS detection circuit



3 Selection of ESD protection device

The transmission rate of USB2.0 FS reaches up to 12 Mbps, and thus TVS array diodes are generally used for ESD protection. When an ESD event arrives, the diode in TVS can be forward-conducted so that the transient current bypasses the sensitive CMOS component and the transient high voltage is reduced to the clamp voltage value in order to protect the interface circuit against ESD damage.

3.1 Clamping voltage

When ESD events are generated, the protection device limits the high voltage pulse to the clamping voltage, and shunts most of the pulse current to the ground in order to protect the back-end sensitive devices. However, there are still some residual current flowing into the protected device. The peak current during ESD event period is the sum of the shunt current passing through ESD protection device and the residual current flowing into the protected device. The power imposed on the protected device depends on the clamping voltage and the residual current.

Clamping voltage can be calculated based on the formula:

Clamping voltage (VCL) = VBR + Io (residual current) x Ro (resistance of the protected device)

For the selection of the clamping voltage of the ESD protection device, the designer must understand which kind of test conditions to be used for determining the value. Based on IEC61000-4-2 Level 4 standard, ESD pulse has the rise time less than 1ns and the duration less than 100 ns, as well as 30A peak current.

ESD protection diode with a clamping voltage of 5V may exceed 30V during the actual ESD test. Without this understanding, the designer may select ESD protection devices according to the minimum clamping voltage in the datasheet.

3.2 Signal integrity

The data transmission system requires that the receptors achieve a certain level of signal integrity. The rise time and fall time of the signal is limited by the impedance of the overall transmission path, along with all parasitic capacitances of the interface. These parasitic capacitances may be introduced by mismatched PCB tracks, USB socket pins or other paralleling capacitances. Therefore it is required that the capacitances of ESD protection devices must be smaller and have the capability to provide ESD protection.

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
2019.08.20	1.0.0	Initial release
2022.3.1	2.0.0	1. Added AT32F435/437/425 to the applicable product list 2. Updated the description of *2 ESD protection design tips*

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