AN0068
Application Note

Hardware connection method between PSRAM/SRAM and XMC

Introduction

This application note provides a hardware method on how to connect 100-pin AT32 MCU to PSRAM/SRAM via XMC interface present on MCU so as to expand storage space.

Applicable products:

MCU	AT32F403Vx
	AT32F403AVx
	AT32F407Vx
	AT32F435Vx
	AT32F437Vx

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1 Overview

Some AT32 MCUs are equipped with an XMC (external memory controller) interface that can be connected externally to PSRAM to expand storage space. Among them, 144-pin MCU supports the connection with nonmultiplexed PSRAM (featuring independent address line and data line), while 100-pin MCU, because of its fewer pins, only supports the connection with multiplexed PSRAM (shared address and data line). At present, nonmultiplexed PSRAM has a price advantage in the market, but AT32 series MCUs are mainly based on 100-pin, which leads to the contradiction in device selection and matching.

Table 1. AT32 MCU and PSRAM selection analysis

MCU pin count	PSRAM type	Advantages	Disadvantages
144	Nonmultiplexed	1. Easy to get PSRAM with lower price; 2.PSRAM operating voltage supports 3.3 V device so that it can be directly connected to MCU.	Only a limited number of MCUs supported (only AT32F403/435/437 are available in 144-pin packages), with lower price
100	Multiplexed	A lot of MCUs for selection and with lower price	1. Not easy to get PSRAM and with higher price 2. PSRAM operating voltage is mainly 1.8V so that an intermediary level is needed to convert voltage to connect to MCU.

If the 100-pin MCU is used, it must be paired with multiplexed PSRAM. But it is hard for the user to accept the high price resulting from the intermediary level that is used to convert voltage for the connection with PSRAM. From this point of view, it seems that 100-pin MCU is unusable. Is there any other way besides selecting 144-pin MCUs? This application note presents a kind of hardware connection approach to cope with the awkwardness, that is, by using two data flip-flops (74LVC574) as the intermediary levels between the100-pin MCU and nonmultiplexed 3.3V PSRAM to handle this issue.

To realize the connection of 100-pin MCU XMC interface with nonmultiplexed PSRAM, it is necessary to add an address latch mechanism to the multiplexed line AD[15:0] to separate an independent address line A[15:0] through NADV signal.

Taking VTI164NA16LM (4M x 16 bits PSRAM) and 74LVC574 (data flip-flop) as an example, this application note describes how to use multiplexed XMC interface to connect to the nonmultiplexed PSRAM.

Note: XMC must be configured in multiplexed mode, and XMC_D[15:0] pin is used as XMC_AD[15:0].

The parallel interface SRAM in the market does not have the multiplexed chip, so it can only be connected to 144-pin package MCU, instead of 100-pin package (not support). The PSRAM is called Pseudo SRAM because it is the disguised SRAM with DRAM technically. Therefore, PSRAM is the same as SRAM in terms of access signal control timing design. The connection between Artery MCU and SRAM is in the same way that it does with the nonmultiplexed PSRAM. The XMC interface on 100-pin MCU can also be connected externally to SRAM by adopting the above connection method and software configuration, just needs to set their respective register value according to chips.

The subsequent descriptions will no longer differentiate nonmultiplexed PSRAM and SRAM because of their identical hardware connection method.

2 Hardware design

2.1 Connection method

PSRAM is mainly operated in asynchronous mode. *Table 2* presents the correspondence between nonmultiplexed PSRAM and XMC interfaces. Regarding to the nonmultiplexed PSRAM, the user needs to connect XMC_AD[15:8] and XMC_AD[7:0] to the D[7:0] pins of two 74LVC574 flip-flops respectively, and connect XMC_NADV to the CLK pins of two 74LVC574 flip-flops in order to separate an independent address line A[15:0] (output by Q[7:0] of the flip-flops) that is connected to the address line A[15:0] pin of the PSRAM. Meanwhile, XMC_AD[15:0] is connected to DQ[15:0] of PSRAM, and the address lines after XMC_A16 and other control lines are directly connected to the corresponding PSRAM pins.

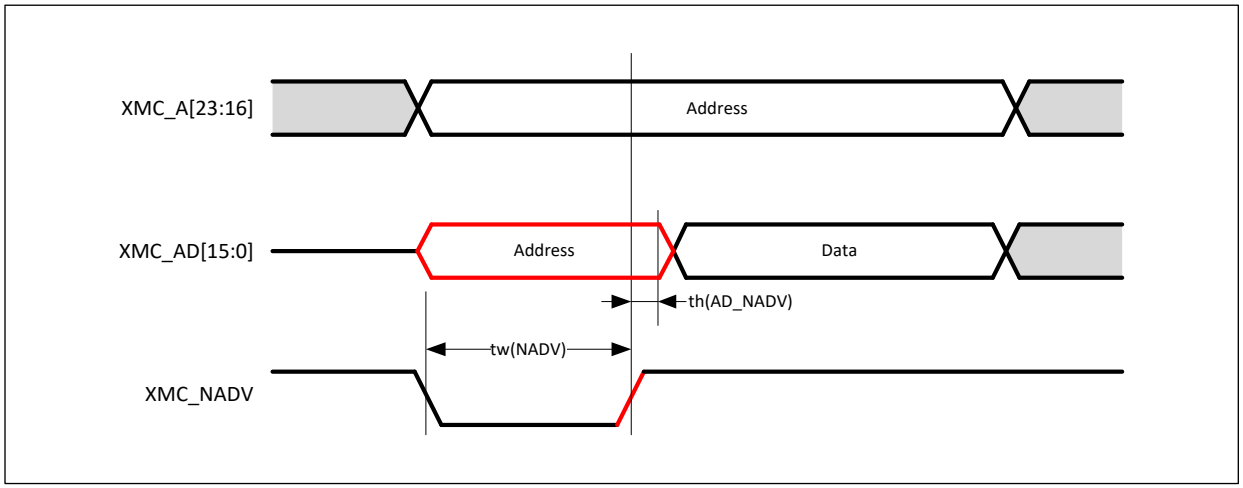
Table 2. XMC, 74LVC574 and PSRAM interfaces

XMC interface	74LVC574 interface	PSRAM interface	Functional description
AD[7:0]	1st D[7:0]	DQ[7:0]	PSRAM return the lower byte data to XMC
AD[15:8]	2nd D[7:0]	DQ[15:8]	PSRAM returns the upper byte data to XMC
-	1st Q[7:0]	A[7:0]	74LVC574 sends the latch lower byte address to PSRAM
-	2nd Q[7:0]	A[15:8]	74LVC574 sends the latch upper byte address to PSRAM
A[n(1):16]	-	A[n(1):16]	XMC sends the address after 16 bit to PSRAM
LB	-	LB#	Lower byte enable
UB	-	UB#	Upper byte enable
NEx(2)	-	CE#	Chip select
NOE	-	OE#	Output enable
NWE	-	WE#	Write enable
NADV	Two CLKs	-	Address valid, the rising edge makes 74LVC574 to latch address

(1) n is subject to PSRAM size. For example, VTI164NA16LM, n = 21.
(2) Available NEx depends on products, and x may range from 1 to 4.

When XMC is configured in multiplexed mode, it will first sent out all address lines, where, A[15:0] is sent via XMC_AD[15:0] port. After the address line is output for a period of time, the address valid signal XMC_NADV will be pulled high before reading to and writing from the data.

Figure1. Address valid signal (NADV) state in memory operation period



Because of the existence of address valid signal NADV, the NADV is used as the CLK of data flip-flop 74LVC574 and can latch the independent address A[15:0] on its rising edge and send it to the non-multiplexed PSRAM.

The 74LVC574 flip-flop can also be replaced with 74HC374 that shares the same function except their respective pin order. 74LVC574 input pin and output pin are placed in the same side of the chip, while 74HC374 pins are staggered. Thus 74LVC574 is recommended for the sake of circuit board layout. Besides, two 74LVC574 flip-flops can also be replaced with one 16-bit data flip-flop, for example, SN74LVTH16374.

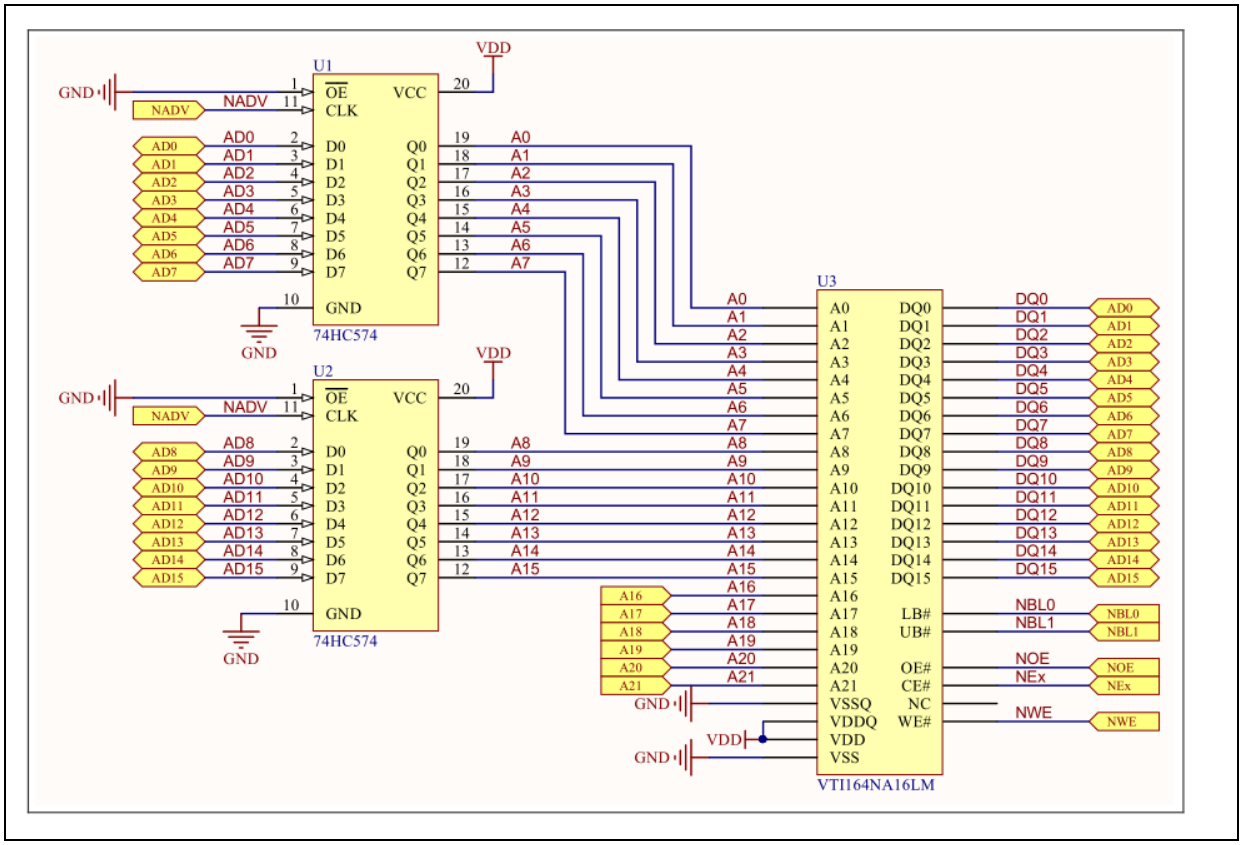
Figure 2. 74LVC574 (data flip-flop) function table

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

2.2 Reference schematic diagram

Figure 3 shows the reference schematic diagram of the hardware connection method. Yellow interfaces are connected to MCU. Some signals have multiple I/Os to select on MCU, depending on the user's application requirements. For available XMC I/Os, please refer to the pin description in the corresponding *AT32 series datasheet.*

Figure 3. Reference schematic diagram



3 Revision history

Table 3 Document revision history

Date	Revision	Changes
2020.06.10	1.0.0	Initial release
2020.07.08	1.0.1	Added the description of the externally-connected parallel SRAM
2021.03.31	1.0.2	Replaced 74HC574 with 74LVC574, because some 74HC574 has longer transmission delay.
2022.2.17	2.0.0	Revised NBL0 to LB, NBL1 to UB.

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