AN0074
Application Note

How to enhance AT32 ADC accuracy

Introduction

This application note describes hardware and software design suggestions as well as precautions regarding the use of ADC module embedded in AT32 MCU.

Applicable products:

MCU	AT32 MCU family

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1 Overview

AT32 microcontrollers embed up to three advanced 12-bit SAR ADCs with self-calibration feature that is used to enhance ADC accuracy in case of changing environmental conditions. In applications involving analog-to-digital conversion, ADC accuracy has an impact on the overall system quality and efficiency. To improve this, it is necessary to gain a better understanding of the ADC operating mechanism and potential factors that may affect its accuracy.

SAR ADC uses a sample capacitor to charge the input signal voltage, which is converted by SAR logic. However, this capacitor is directly charged with external signal source, coupled with the impact of the sample capacitor value, input impedance and external circuits, so it needs to wait a period of time until the charge becomes stable in order to ensure the accuracy of input signal voltage measured. To achieve ADC accuracy, enough sample time must be configured. Otherwise, the residue charge on the sample capacitor left by the previous conversion on certain input channel will have an effect on the accuracy of on-going conversion channel. ADC accuracy does not only depends on ADC performance and features but also on the overall application design around the ADC.

This application note aims at helping users understand how to enhance ADC accuracy through hardware and software methods, as well as providing precautions on related applications.

2 ADC errors

This section lists the main errors that have an impact on ADC conversion accuracy. These types of errors are common to all AD converters and the conversion quality depends on their elimination. For easy reference, accuracy errors are expressed in the unit of LSB. In terms of voltage, the voltage error is calculated by multiplying the number of LSBs by the voltage corresponding to 1 LSB (1 LSB = V_{REF+} / 4096 or V_{DDA} / 4096)

2.1 Errors due to ADC itself

These errors result from the ADC design and manufacturing process. They are usually shown by the following static parameters: differential linearity error (DNL), integral linearity error (INL), offset error (OE), gain error (GE) and total unadjusted error (TUE). The definitions and values of these errors are specified in AT32 microcontroller datasheet. The total unadjusted error (TUE) is the maximum deviation between the actual and the ideal transfer curves. This parameter specifies the maximum deviation between the ideal digital output and the actual digital output that may occur. (Please be noted that the TUE is not the sum of DNL, INL, OE and GE, but may result from one more errors occurring simultaneously)

AT32 ADC self-calibration function can compensate the offset error. Performing ADC self-calibration before starting analog-to-digital conversion can make sure that the TUE is lower than 4 LSB, that is, 12-bit ADC static accuracy reaches over 10 bit following the environmental conditions specified by AT32 microcontroller datasheet.

The ADC dynamic parameters (such as ENOB) and their respective errors are mainly involved in the voice and specific audio applications instead of general MCU applications, so they are not included in this document.

2.2 Errors due to ADC environment

2.2.1 Reference voltage/power supply noise

As the ADC output is the ration between the analog signal voltage (V_{AIN}) and the reference voltage (V_{REF+}), any noise on the V_{REF+} causes a change in the converted digital value. In some packages, V_{DDA} analog power supply is used as the reference voltage (V_{REF+}), so the quality of V_{DDA} power supply has an impact on ADC error. A fluctuation of dozens of mV on V_{REF+} would cause an error of a dozen of LSBs.

In terms of power supply noise, the switching power supply module usually embed a fast-switching power transistor, which causes high-frequency noise during output. This switching noise is between 15 kHz and 1 MHz. Linear regulators have a better output quality. If you are using a switching power supply, it is recommended to use a linear regulator to supply the analog stage. It is recommended to connect capacitors with good high-frequency characteristics between the power and ground lines. In other words, a 0.1 µF and a 1 to 10 µF capacitor should be placed close to the power supply. These capacitors allow the DC signals to pass through them. The small-value capacitors filter high-frequency noise and the high-value capacitors filter low-frequency noise. To filter high-frequency noise, a ferrite inductor in series with the power supply can also be used. As the series resistance of the wire is very low, this solution leads to very low (negligible) DC loss unless the current is high. The V_{DD} and V_{SS} pins are placed close to each other, and thus a capacitor can be connected very close to the microcontroller with very short leads. V_{DDA} and V_{REF+} pins must be connected to two external decoupling capacitors: 100 nF ceramic capacitor + 1 µF Tantalum or ceramic). It should be noted that the digital ground and analog ground must be

separated each other to avoid cross noise.

Figure 1. Power supply and reference decoupling for packages with V_{REF} pins

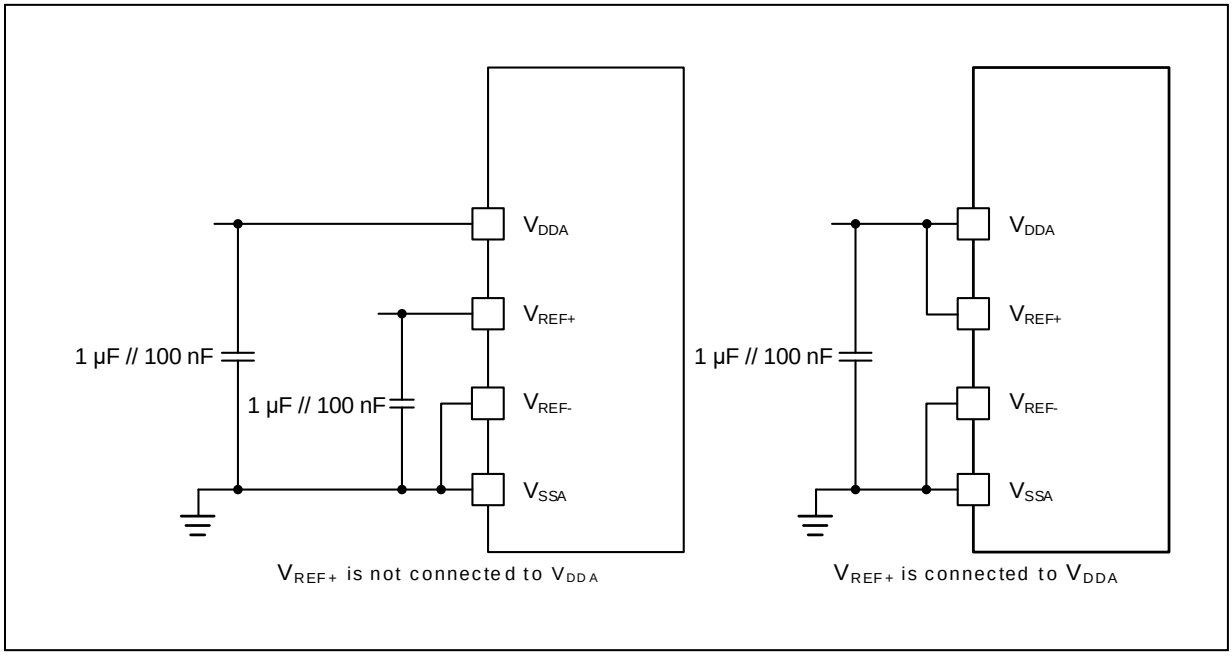
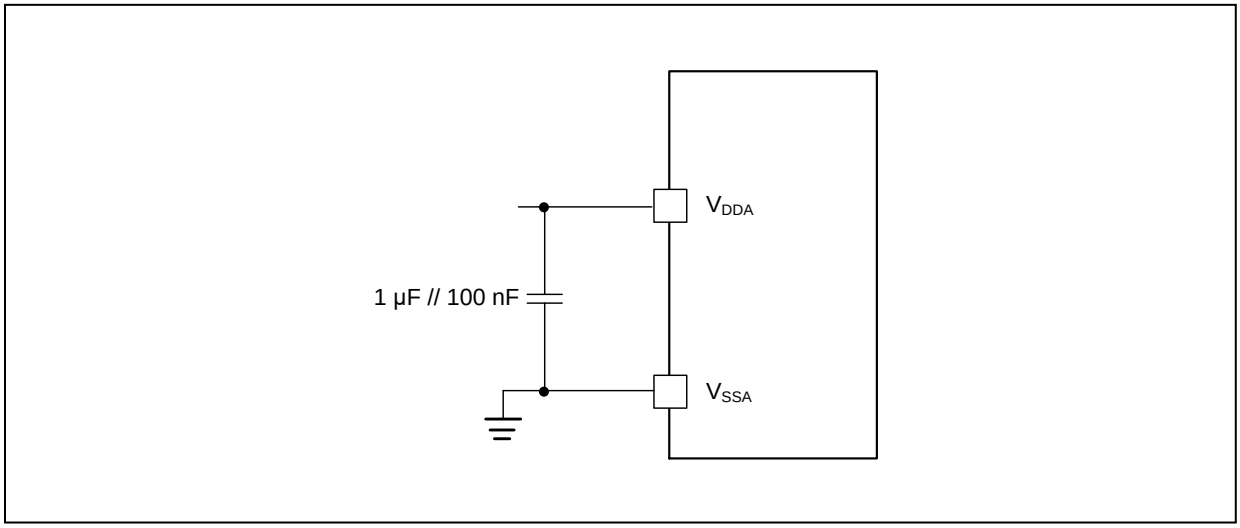


Figure 2. Power supply and reference decoupling for packages without V_{REF} pins



2.2.2 GPIO input voltage is out of normal range

For AT32F403, AT32F413 and AT32F415 series, the input voltage to any GPIO pin with ADC input features is not allowed to exceed V_{DD} + 0.3 V (V_{DDA} and V_{DD} must be at the same potential), otherwise, the ADC input signals could be interfered internally. For the GPIO with ADC input features, even if it is only used as I/O input, if the input voltage exceeds V_{DD} + 0.3 V, it would also affect other ADC channel conversion results. If there is such a high voltage, it is recommended to use resistances to divide or reduce the voltage to the range within V_{DD}.

Other AT32 series MCUs (such as, AT32F403A and AT32F421 series) are not subject to the above-mentioned limits because their GPIO pins with ADC input features are all 5V tolerant. When these pins are used as digital input instead of ADC input signals, they need to be set as input floating, input pull-up or input pull-down mode so that the voltage higher than V_{DD} can be input without

interfering ADC operations. However, t the input voltage must not exceed 5.5 V.

Inputting a negative voltage on the GPIO pin also affects the ADC conversion accuracy, so the input voltage must not be lower than -0.3 V.

2.2.3 Analog input signal noise

Small but high-frequency signal changes can result in big conversion errors during sampling time. This noise is generated by electrical devices (such as, motors, engine ignition and power lines). It affects the analog input source signal (such as sensors) by adding an unwanted signal. As a result, ADC conversion results are not accurate.

Averaging method

Averaging is a simple technique where you sample analog input several times and take the average of the results by software. This technique is helpful to eliminate the noise on the analog input in case of an analog voltage that does not change often. If an instable ADC value generated on the measured analog signal, the software can delete the maximum and minimum values to select an appropriate number of samples to perform averaging. The number depends on the required accuracy and minimum conversion speed.

The advantage of this averaging method is to enhance ADC accuracy without changing hardware, while its disadvantage lies in its slow conversion speed and frequency response, which is equivalent to the reduction of effective sampling frequency.

Adding an external filter

Adding an external RC filter eliminates the high frequency. An expensive filter is not needed to deal with a signal that has frequency is higher than the frequency range involved. In this case, a relatively simple low-pass filter with a cut-off frequency fc just above the frequency range involved is enough to limit noise and aliasing. A sampling rate consistent with the highest frequency involved is enough, usually two to five times fc.

However, when an extern RC filter is added, the ADC sampling time and sampling interval need to be re-evaluated, otherwise it may cause greater measurement errors. For more information, please refer to *Section 3*

2.2.4 Effect of the analog signal source resistance

The impedance of the analog signal source, or series resistance (R_{AIN}), between the source and pin, causes a voltage drop on it because of the current flowing into the pin. The time required to fully charge the hold capacitor is increased. If the sampling time is less than the time required to fully charge the internal sampling capacitor, there will be an offset between ADC digital value and the actual value.

Refer to *Section 3* for more information on ADC measurement configuration when the analog signal source has high input resistance characteristics or is added with RC filter.

2.2.5 Internal CPU noise

When the CPU (and other peripherals) operates, it generate a lot of internal and external signal changes which are transferred to the ADC peripheral through capacitive coupling. This disturbance affects ADC precision.

To minimize the impact of the CPU (and other peripherals) on ADC, it is necessary to minimize the digital signal changes during sampling and conversion time (digital silence). This is done by using one of the following methods (implemented during sampling and conversion time)

- minimize internal CPU changes (CPU stop, wait mode)
- stop clock for unnecessary peripherals (timers, communications…)

2.2.6 Temperature influence

The temperature has a major influence on ADC accuracy. It mainly generates two major errors: offset error drift and gain error drift. It is recommended to use internal temperature sensor and ADC watchdog to re-calibrate ADC when the temperature changes reach a given value.

2.2.7 I/O pin crosstalk

Switching I/O may generate some noise in the analog input of the ADC due to capacitive coupling between I/Os. The PCB trace that run close to each other or that cross each other may introduce crosstalk. Internally switching digital signals and I/Os leads to high-frequency noise. Switching high-sink I/Os may induce some voltage drops in the power supply due to current surges.

A digital trace that crosses an analog input trace on the PCB may affect the analog signal. The noise produced by crosstalk can be reduced by shielding the analog signal by placing ground trace on it. When placing PCB trace, you should consider to shield ADC input signal. This is done by coating the signal trace with copper and making it grounded nearby, and shortening the wiring distance as much as possible. Besides, minimizing the I/O pin changes during ADC sampling and conversion time is helpful to reduce the disturbance on ADC.

2.2.8 EMI-induced noise

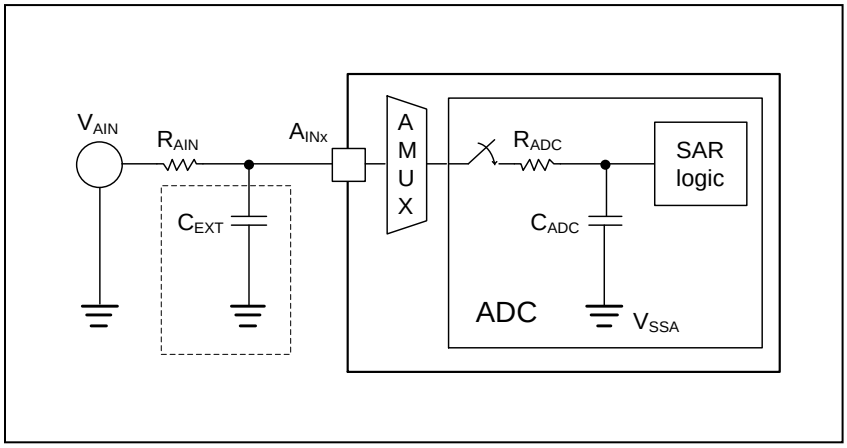
Electromagnetic emissions from neighboring circuits may introduce high-frequency noise in the analog signal because the PCB traces may act like an antenna to receive the noise. The user can reduce EMI noise by physically separating the sources of emission from the receptors, or electrically separating by proper grounding and shielding.

Placing ground traces alongside sensitive analog signals provides shielding on the PCB. The other side of the two-layer PCB should also have a ground plane to prevent interference and I/O crosstalk from affecting the signal. Signals coming from distant locations (such as sensors) should be connected to the PCB using shielded cables. It should be noted that the length of the paths of these signals on the PCB should be minimized as much as possible. Crystal, clock and the signal traces that fast change should separate from ADC input signals as much as possible.

3 Effect of ADC input source resistance on the measurement

SAR ADC measurement requires enough sampling time to fully charge and discharge ADC internal sampling circuits to obtain conversion accuracy. This is also true to multi-channel conversions. Sufficient sampling time can avoid crosstalk between input channels. To calculate the estimated sampling time, Figure 3 shows a circuit diagram that approximates the equivalent resistance and capacitance of the ADC sampling circuit (including analog multiplexer, analog switch, parasitic capacitance, sampling capacitor…)

Figure 3. ADC simplified diagram of input stage - sample and hold circuit

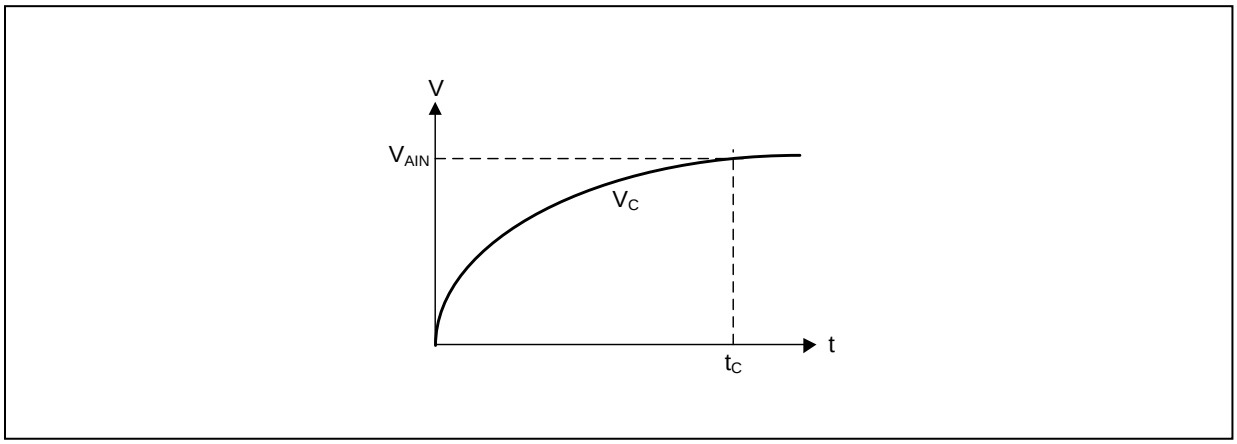


Among them, the input resistance (R_{AIN}) of the analog signal source to the ADC is directly related to the ADC sampling time, having an important impact on the ADC conversion results. If the input resistance is not considered, the external devices of ADC input are inconsistent with the sampling time set by software, resulting in ADC errors often. The following sections describes how to set ADC software and hardware properly based on the signal source featuring general input resistance or high input resistance.

3.1 General input impedance measurement

Vc is the voltage across the internal C_{ADC} capacitor (*Figure 4).* For a given sampling $t_{C,}$ you should consider to take the maximum sampling time t_C corresponding to $V_{AIN} = V_{REF+}$ because C_{ADC} needs the most time to be charged from 0 V to V_{AIN} at this time. Therefore, $V_{AIN} = V_{REF}$ is the worst case to verify when the source resistance is maximum. The sampling time can be increased by software or reducing ADC clock frequencies. The longer the sampling time, the better the conversion results.

Figure 4. Schematic diagram of analog signal source charging sample and hold circuit



Typically, we assume that the maximum allowable error equals to 1 LSB. Following RC charge and discharge formula:

$V(t) = V_{AIN} \times (1 - e^{-t/\tau})$

$t = \ln\left(1 - \frac{V_{AIN}}{V(t)}\right) \times \tau$

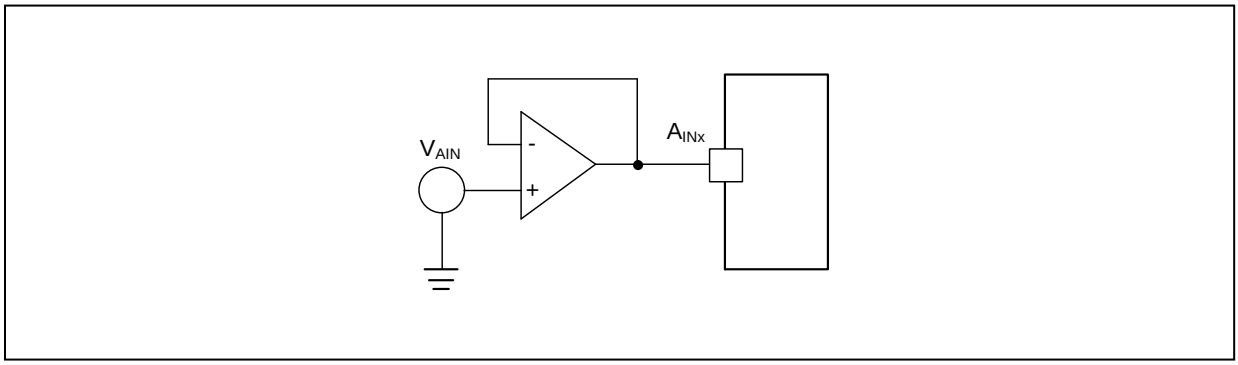
Where, V (t) is replaced with $V_{REF} \times \left(1 - \frac{1}{2^{12}}\right)$, V_{AIN} with V_{REF}, and $\tau = (R_{AIN} + R_{ADC}) \times C_{ADC}$

If the sampling time is larger than 8.32 x (R_{AIN} + R_{ADC}) x C_{ADC}, the error is within 1 LSB. If the user requires a lower accuracy, they can further increase the allowable external resistance RAIN.

3.2 High impedance measurement

ADC input signal sources have usually high-impedance characteristics. For example, the system battery voltage, after being divided, is input to ADC sampling. But because the voltage divider forms a DC power consumption path, it is often combined with a resistance value ranging from 100 kΩ to 1 MΩ to save power. Another case, some sensors have weak current output, which is converted into voltage by connecting to a large resistor externally. Thus it is impossible for the hardware to debug an appropriate sampling time using above-mentioned methods (for example, it is unable to get accurate conversion results even though the sampling time is the maximum by software, or reducing ADC clock frequency causes the overall sampling time to be too long). In this case, an operational amplifier can be added in front of the ADC input channel to strengthen input driving force, as shown in *Figure 5*. This solutions can significantly shorten the ADC sampling time and sampling interval but would increase component costs. More than that, additional errors, such as extra offset, amplifier gain stability or linearity and frequency response, may happen when designing the pre-amplifier, which will become the source for other measurement errors if the amplifier is not selected properly.

Figure 5. Schematic diagram for adding operational amplifier before ADC input channel



If the hardware circuit does not support the operational amplifier, it is impossible to shorten the sampling time using this method. In this case, an external capacitor can also be used as the charge memory.

After the sampling switch is turned on, the internal sampling and hold capacitor of SAR ADC need a sufficient amount of charge and discharge current during the stable time. But the actual signal circuit usually has high input impedance, so it is unable to provide big enough current to quickly charge the ADC sampling capacitor. To this end, most applications adopt an external large capacitor as a charge memory to connect the ADC input pin to the ground, that is, C_{EXT} in *Figure 3*. Such capacitor takes part in the charge and discharge process of the sampling circuit so as to supply enough current for SAR ADC sampling capacitor, while quickly charges the internal sampling capacitor, and stabilize the voltage at ADC input point. The RC filter composed of C_{EXT} and $R_{AIN\ also}$ limits the noise arriving on ADC input, while helps reduce the kick-back effect resulting from the switch capacitor frequent switching and on-offs at ADC input end. Of course, such RC filter also limits the cut-off frequency of V_{AIN} signal source.

Calculate the C_{EXT}

When the sampling switch is turned on, there will be a charge redistribution process between C_{EXT} and $C_{ADC,}$ in which, RC time constant is mainly determined by the maximum R_{ADC} and maximum $C_{ADC.}$

In considering the charge distribution between C_{EXT} and $C_{ADC,}$ the C_{PAD} can be ignored because it is relatively small and in series with $C_{EXT.\ The\ formula\ of}$ the charge distribution is based on the fact that the total charge before distribution is equal to the total charge after distribution.

Assume that C_{ADC} is fully discharged, and C_{EXT} storages the same voltage as V_{AIN}. V_C (allocated voltage) is defined as 0.999939 times of $V_{AIN,}$ meaning that the final V_C offset is within 1 LSB of V_{AIN} based on 12-bit resolution.

$$V_{AIN} \times \left(1 - \frac{1}{2^{12}}\right) = \frac{C_{EXT} \times V_{AIN} + C_{ADC} \times 0}{C_{EXT} + C_{ADC}}$$

$$C_{EXT} = 4095 \times C_{ADC}$$

For example, C_{ADC} = 15 pF,

C_{EXT} = 4095 x 15 pF = 61.4 nF

This is the absolute minimum value of C_{EXT}. It is necessary to take into account the device differences and aging factors when selecting the device value. It is allowed to choose a little bit large value, such as 68 nF. If the capacitance value is even larger, it is actually not helpful to the reduction of sampling time but only limits the bandwidth of the ADC input signal.

But if a 12-bit ADC is configured as $C_{EXT} < 4095 \times C_{ADC}$, a large amount of sampling time is needed to fully charge the C_{ADC} instead. Thus if $C_{EXT} < 4095 \times C_{ADC}$ and the user does not need anti-aliasing filter, it is not recommended to add C_{EXT}.

If the required accuracy is not so high, C_{EXT} can be reduced according to the above formula, and the bandwidth of the ADC input signal is increased accordingly. Otherwise, the C_{EXT} value must be increased, but at the expense of the increased ADC sampling time and the reduced bandwidth of ADC input signal.

Calculate R_{AIN}

The sum of all resistance charging the external capacitor C_{EXT} is R_{AIN}, that is, the equivalent resistance of the driving signal source as seen from C_{EXT}. When R_{AIN} becomes larger, the cut-off frequency formed by R_{AIN} and C_{EXT} would become lower, indicating that the time duration from the input signal starts changing to C_{EXT} charge stability would increase.

To make sure that the accuracy error is within 1 LSB based on 12-bit resolution, the time constant of RC circuit is required as:

$\ln(2^{12}) = 8.32$ Times

The cut-off frequency by Cext and Rain:

$$f = \frac{1}{8.32 \times R_{AIN} \times C_{EXT}}$$

Taking the previous C_{EXT} = 62 nF as an example, if R_{AIN} = 200 Ω, the cut-off frequency can reach 9.7 kHz; if R_{AIN} = 20 kΩ, only allow 97 Hz. The ADC conversion result is not accurate if the frequency of the source exceeds the above cut-off frequency.

Note that ADC must be configured in single-point mode or trigger conversion at a timer interval, instead of being set in continuous mode, and the software must ensure that the time interval between two conversions must be equivalent to or larger than 1/f.

Consequences due to insufficient sampling time

If a big enough C_{EXT} is placed in ADC input according to C_{EXT} calculation formula, the time to stabilize C_{ADC} becomes very short. There is only one exception that the C_{EXT} is not needed when R_{AIN} is very small. Generally speaking, R_{AIN} is very small because the sensor has an output buffer stage, so R_{AIN} is lower than 100 Ω at this time. The sampling time can be met under above situations.

Insufficient sampling time causes crosstalk among ADC channels. As mentioned at the beginning of this document, the charge from one channel is accumulated on C_{ADC} and transferred to another channel, which results in crosstalk between channels.

Consequences by signal source high impedance

The reason to this crosstalk is that the input impedance of the signal source is too high. To achieve the accuracy of 1 LSB, it is necessary to add a delay during the channel conversion, with the

consequence being that the overall conversion time becomes slow.

If there is no C_{EXT} or the capacitor is too small, along with insufficient sampling time, the ADC conversion result would never reach 1 LSB accuracy because of crosstalk among channels.

3.3 Suggestion on input impedance match

As the ADC design tends to focus on low-power, high sample frequency and complex features, the ADC sampling behavior cannot longer be simulated using simple R_{ADC} and C_{ADC} model. Thus more and more ADC specifications only come with typical C_{ADC} value, without R_{ADC} value, which has been replaced with the correspondence between ADC input signal resistance (R_{AIN}) and sampling time (ts), as shown in the table below (from AT32F403A datasheet).

Table 1. Maximum R_{AIN}(1) when f_{ADC} = 28 MHz

T_S (period)	t_S (μs)	Max R_{AIN} (kΩ)
1.5	0.05	0.1
7.5	0.27	0.6
13.5	0.48	1.2
28.5	1.02	2.5
41.5	1.48	4.0
55.5	1.98	5.2
71.5	2.55	7.0
239.5	8.55	20

(1) Guaranteed by design.

When the input impedance of the ADC signal source is available, the user simply follows this table to set sufficient time through software so as to get a reasonable ADC conversion result without calculation. In most cases, the user cannot get the impedance of ADC signal source, directly or indirectly, so the best method is to gradually debug software sampling time.

Using the following procedures to debug ADC sampling time:

(1) Configure ADC clock frequency as maximum, and the sampling period as maximum;

(2) Try ADC conversion and review the conversion result;

(3) If the conversion value meets the expectation, you can gradually reduce the sampling period and watch ADC conversion value to get enough but not too long sampling time;

(4) If the conversion value based on maximum sampling time is out of expectations, the user needs to reduce ADC clock frequency or follow the previous formula and add an appropriate $C_{EXT;}$ Hardware configuration is followed by the software configuration to gradually get appropriate sampling time and sampling interval.

In addition, if the sampling interval and time permit, using some software tips also help enhance ADC conversion accuracy, such as:

(1) Averaging method, moving average method or median filtering;

(2) For sampling twice the same ADC channel, disregard the first sampling value and use the second one. This solution can help eliminate the effect of the accumulated charge when sampling is switched between different channels, the voltage from the last channel is too late to discharge from the sampling resistance because of excessive input source impedance,

which will influence the conversion value of the next channel.

(3) If ADC input signal is between 0 V and $V_{REF+}/2$, it is possible to convert this ADC input channel and internal V_{INTRV} alternately, and make the sampling resistance have enough time to discharge and charge so as to avoid crosstalk among channels. If there is an internal V_{SSA} channel, it is much better and time-saving to convert ADC input channel and internal V_{SSA} channel, because it takes less time of discharging ADC sampling circuit to V_{SSA} than charging and discharging ADC sampling circuit to V_{INTRV}.

4 Other application notes on ADC

4.1 Internal reference voltage V_{INTRV} configuration

Internal reference voltage (V_{INTRV}) provides a stable voltage output for ADC. It is connected to ADC1_IN17 input channel internally for converting V_{INTRV} output to a digital value.

V_{INTRV} is a constant voltage signal source inside the chip. Based on the spec 1.2 V±3.3 %, it is maintained within this spec in all V_{DDA} operating voltage ranges, and does not change with V_{DDA} voltage. Therefore, when the external V_{REF}+ voltage (usually share the same power supply with V_{DDA}) of ADC is not available or when V_{VREF+} voltage changes (such as, using a battery), the user can refer to V_{INTRV} to calculate V_{REF+} or V_{DDA} voltage and accurate absolute voltage of each ADC_IN input.

For example, If the selected V_{INTRV} channel, after ADC conversion is 1650 (Code_V_{INTRV}), you can conclude that the V_{REF+} or V_{DDA} at full charge is 1.2 x 4096 / 1650 = 2.979 V. In this case, if the value converted by another selected ADC_IN external channel is 800 (Code_V_{AIN}), you can use the following formulas: 1.2 x 800 / 1650 or 2.979 x 800 /4096, the external signal voltage V_{AINx} is calculated at 0.582 V.

Formulas involved in the above example:

V_{REF+} or V_{DDA} = (V_{INTRV}) x 4096 / (Code_V_{INTRV})

V_{AINx} = (V_{INTRV}) x (Code_V_{AIN}) / (Code_V_{INTRV})

V_{AINx} = V_{REF+} or V_{DDA} x (Code_V_{AIN}) / 4096

The user can determine the conversion times and conversion interval of V_{INTRV} according to the features of the power supply of the applications. If the voltage of the power supply is unknown but unchanged, after the system power-on, the user can initialize ADC and calibrate to finish V_{INTRV} conversion at one time; If the voltage of the power supply is of variable voltage, the user can determine the V_{INTRV} conversion interval based on the power supply change speed and system requirements, and conduct several times of V_{INTRV} conversion and update the reference value, and even need re-calibrate ADC. In addition, the temperature changes also may affect power supply situations. Also you can refer to *section 2.2.6* to launch V_{INTRV} conversion.

The V_{INTRV} is an internal weak voltage source, so ADC sampling time must be sufficient to for V_{INTRV} to discharge and charge the sampling circuit. The user should follow the T_{S_INTRV} parameters described in the datasheet to set up enough sampling time for V_{INTRV} to get the accurate conversion value.

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
2020.10.9	1.0.0	Initial release
2020.10.22	1.0.1	Added *Section 4 Other application notes on ADC*
2022.2.24	2.0.0	*1. Added 2.2.2 GPIO input voltage is out of normal range* *2. Changed* V_{REFINT} *to* V_{INTRV}

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