

### AN0129

**Application Note** 

## Getting Started with AT32F425

## Introduction

This document is aimed at helping users with project development based on AT32F425xx MCUs.

Note: The corresponding code in this application note is developed on the basis of V2.x.x BSP provided by Artery. For other versions of BSP, please pay attention to the differences in usage.

Applicable products:



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## 1 Development resources

#### **Resources download link:**

Visit Artery website: <u>https://www.arterychip.com</u>

## 1.1 Set up AT32 development environment

## 1.1.1 Debug tools and evaluation board

The AT32F425 evaluation board comes with AT-Link-EZ for the debug purpose, as shown in the left red box of the figure below. It can also be disassembled from the evaluation board and used separately with other circuit boards. This debug tool can be used for several purposes such IDE online debugging, online programming and USB-to-serial interface.



Figure 1. AT\_START\_F425 and AT-Link-EZ

Note: For details on AT-START-AT32F425 evaluation board, refer to the "UM\_AT\_START\_F425\_Vx.x", which is available from <u>ARTERY official website</u>  $\rightarrow$  Product  $\rightarrow$  Value line  $\rightarrow$  AT32F425 series  $\rightarrow$  Resources  $\rightarrow$  Evaluation Board (download and unzip, and then go to "VAT\_START\_F425\_Vx.x\03\_Documents").

#### Figure 2. AT-START-F425 evaluation board package from ARTERY official website

valuation Board		
Download	Description	Version
AT-START-F425	AT32F425 evaluation board supporting Arduino standard interfaces	V1.00

## 1.1.2 Programming tools and software resources

AT programming tools and software: AT-Link / AT-Link+ /AT-Link-Pro / AT-Link-ISO /AT-Link-EZ, and ICP/ISP



Third-party programming tools: J-Link, Armfly, Alientek, XWOPEN, ICWORKSHOP, ZLG, MaxWiz, Amomcu, Acroview, Forcreat, Galecomm, Prosystems, Rx-prog, Sinaen, XELTEK, and Zhifeng

Note: These programming tools are available from <u>ARTERY official website</u>  $\rightarrow$  Support $\rightarrow$  Hardware Development Tool or 3<sup>rd</sup> Party Writer.

- ICP user guide: Refer to the UM\_ICP\_Programmer, which is available from <u>ARTERY official</u> <u>website</u> → Products → Value line → AT32F4xx → Tool → ICP (download and unzip, and then go to Artery\_ICP\_Programmer\_Vx.x.xx\Document\UM\_ICP\_Programmer)
- ISP user guide: Refer to the UM\_ISP\_Programmer, which is available from <u>ARTERY official</u> <u>website</u> → Products → Value line → AT32F4xx → Tool → ISP (download and unzip, and then go to Artery\_ISP\_Programmer\_Vx.x.xx\Document\UM\_ISP\_Programmer)
- AT-Link user guide: Refer to the UM0004\_AT-Link\_User\_Manual, which is available from <u>ARTERY official website</u> → Products→Value line→AT32F4xx→Tool→AT-Link-Family (download and unzip, and then go to AT\_Link\_CH\_ Vx.x.x\05\_Documents\UM0004\_AT-Link\_User\_Manual\_EN\_Vx.x.x)

#### Figure 3. ICP/ISP/AT-Link-Family package on ARTERY official website

Download	Description	Version
AT32 IDE_Linux AT32 IDE_Windows	A software development environment for cross-platform ARM embedded system based on Eclipse development supporting AT32 MCU	V1.0.05
📥 AT-Link	Emulation and online/offline programming tools supporting AT32 MCU	V2.1.1
AT-Link Console_Linux AT-Link Console_Windows	In-Circuit-Programming Console tool supporting AT32 MCU	V3.0.06
🛓 ICP	In-Circuit-Programming tool supporting AT32 MCU	V3.0.09
🛓 ISP	In-System-Programming tool supporting AT32 MCU	V2.0.09
▲ ISP_Multi-Port	In-System-Multi-Port Programming tool supporting AT32 MCU	V2.0.09
▲ ISP Console_Linux ▲ ISP Console Windows	In-Circuit-Programming Console tool supporting AT32 MCU	V3.0.06

## 1.1.3 AT32 development environment

### 1.1.3.1 Template project

The frequently-used IDE template projects are included in ARTERY's firmware BSP. You can get these resources by visiting <u>ARTERY official website</u>  $\rightarrow$  Products  $\rightarrow$  Value line  $\rightarrow$  AT32F425 series  $\rightarrow$  BSP.

BSP	
Download	Description
🛓 Firmware Library	AT32F425 firmware library BSP user guide

#### Figure 4. BSP resources on ARTERY official website



BSP offers such template projects as *Keil\_v5/Keil\_v4/IAR\_6.10/IAR\_7.4/IAR\_8.2/eclipse\_gcc* /*at32\_ide*, which are stored at AT32F425\_Firmware\_Library\_V2.x.x\project\at\_start\_f4xx \templates.

Just simply open the desired folder and IDE project. Figure 5 below shows an example of Keil\_v5 project.



Figure 5. Keil\_v5 templates template

This template mainly contains the following items:

- at32f425\_clock.c: clock configuration file, which defines the default clock frequency and clock path
- ② at32f425\_int.c: interrupt file, which contains the default process of handling some core interrupts
- ③ main.c: main code file
- (4) **at32f425\_board.c**: board configuration file, which defines common hardware such as buttons and LEDs on AT-START evaluation board
- (5) firmware: it contains "at32f425\_xx.c" that is used as a driver file for peripherals
- 6 system\_at32f425.c: system initialization file
- ⑦ startup\_at32f425.s: startup file
- (8) **readme.txt**: a read-me txt file that describes some application functions, configuration method and application notes relating to a template project.

In addition to "Templates", a large number of examples are included in BSP for users' reference. These example codes are stored at:

AT32F425\_Firmware\_Library\_V2.x.x\project\at\_start\_f4xx\examples.

Note: For details on BSP, refer to Section 4 of the document "AT32F425\_firmware\_BSP&Pack\_user\_guide", which is available from <u>ARTERY official website</u>  $\rightarrow$  Products $\rightarrow$  Value line $\rightarrow$ AT32F425 series $\rightarrow$ BSP (download and unzip, and then go to "\AT32F425\_Firmware\_Library\_Vx.x.x\document").

### 1.1.3.2 Pack installation

The installation of Pack is required to add AT32 MCU part number in Keil/IAR.

The Pack is available from <u>ARTERY official website</u>  $\rightarrow$  Products  $\rightarrow$  Value line  $\rightarrow$  AT32F425 series.



#### Figure 6. Pack resources on ARTERY official website

Download	Description
<ul><li>▲ Keil 4</li><li>▲ Keil 5</li></ul>	Supports AT32 MCU to run in Keil MDK
🕹 IAR	Supports AT32 MCU to run in IAR EWARM
🕹 Segger	Supports Segger tools to identify AT32 MCU
🕹 ConfigJLink	How to resume download for AT32 series

For the Keil compiling system, Keil 4.74, Keil 5.23 and above versions are recommended.

For Keil\_v5, users need to unzip the "*Keil5\_AT32MCU\_AddOn*" and then install the "*ArteryTek.AT32F425\_DFP*".

For Keil\_v4, users directly install the "Keil4\_AT32MCU\_AddOn".

By default, the installation path of Keil can be automatically recognized when installing. In case of recognition failure, users need to manually select the Keil installation path.

#### Figure 7. Install ArteryTek.AT32F425\_DFP

Pack Unzip: ArteryTek AT32F425_DFP 2.0.2			×
Welcome to Keil Pack Unzip Release 4/2022			
This program installs the Software Pack: ArteryTek AT32F425_DFP 2.0.2 ArteryTek AT32F425 Series Device Support.Drivers			
Destination Folder	0.2		
Keil Pack Unzip	<< Back	Next >>	Cancel

#### Figure 8. Install Keil4\_AT32MCU\_AddOn

Setup AT32 MCU AddOn Package to Keil MDK-ARM V2.1.0	– 🗆 X
Folder Selection Select the folder where SETUF will install files	ARM <sup>®</sup> KEIL <sup>®</sup> Microcontroller Tools
This Add-On will install into the following product folder. To install to this folder, press"Next", To install to a differ press "Browse" and select another folder. Destination Folder [D:\Keil_y4]	nt folder, Browse
-Keil MDR-ARM Setup	Next >> Cancel



Users can also open Keil $\rightarrow$ click "Pack Installer" $\rightarrow$ click "File" $\rightarrow$ choose "Import" to import the corresponding pack downloaded from <u>ARTERY official website</u>.

Figure 9. Click "Pack Installer" in Keil



For the IAR compiling system, IAR7.0, IAR6.1 and above versions are recommended.

By default, when installing the "*IAR\_AT32MCU\_AddOn*", the installation path of IAR can be automatically recognized. In case of recognition failure, users need to manually select the IAR installation path.

Figure 1	10.	Install	IAR_	_AT32MCU	_AddOn
----------	-----	---------	------	----------	--------

😹 Setup AT32 MCU AddOn Package to IAR V2.0.8	×
This SETUP program installs: AT32 MCU Device AddOn Package to IAR	
This AddOn will install into the following product folder. To install to this folder,press "Start". To install to a different folder, press "Browse" and select another folder.	
Destination Folder D:\Program Files (x86)\IAR Systems\Embedded Workbench 8.2	Browse
Realtime Status 0%	Cancel

Note: For details on Pack, refer to Section 2 of the document "AT32F425\_firmware\_BSP&Pack\_user\_guide", which is available from <u>ARTERY official website</u>  $\rightarrow$  Products $\rightarrow$  Value line $\rightarrow$ AT32F425 series $\rightarrow$ BSP (download and unzip, and then go to "\AT32F425\_Firmware\_Library\_Vx.x.x\document").

### 1.1.3.3 Debug and download with AT-Link tool

If AT-Link is to be used in Keil environment, click "Debug", and then choose "CMSIS-DAP Debugger".



📚 🖾 🕮 🥪 🔜   鞲   template										
Project 🛛 🕂 💌	main.c									
<ul> <li>Project: template</li> <li>template</li> <li>template</li> <li>user</li> </ul>	Options for Target 'template'     X      Device Target (Dutput Listing User   C/C++   Asm   Linker Debug   Utilities									
	C Use Simulator <u>with restrictions</u> Settings □ Limit Speed to Real-Time ULINK2/ME Contex Debugger A ULINK2/ME Contex Debugger A	Settings								
e- 🖢 bsp ⊕- 🗋 at32f425_board.c ⊕- 📴 firmware	✓ Load Application at Startup     ✓ Run to main()     ✓ Load CMSIS-DAP Debugger	Edit								
<ul> <li>cmsis</li> <li>system_at32f425.c</li> <li>startup_at32f425.s</li> </ul>	Restore Debug Session Settings     Restore Stellars (CD)       Image: Stellars (CD)     Image: Stellars (CD)       Image: Stellars (CD)									
- 🧀 readme	Image: The state of									
	CPU DLL: Parameter: Driver DLL: Parameter:									
	SARMCM3.DLL -REMAP -MPU SARMCM3.DLL -MPU									
	Dialog DLL: Parameter: Dialog DLL: Parameter:									
	DCM.DLL pCM4 TCM.DLL pCM4									
	Manage Component Viewer Description Files									

Figure 11. Keil Debug option

Next, click "Settings" to enter "Cortex-M Target Driver Setup" window, as shown in Figure 12 below.

1. Select "AT-Link(WinUSB)-CMSIS-DAP/AT-Link-CMSIS-DAP";

Note: For more information on WinUSB, refer to "FAQ0136\_How\_to\_use\_AT-LINK\_WinUSB\_EN\_V2.0.0", which is available from <u>ARTERY official website</u> $\rightarrow$ Support $\rightarrow$ FAQ $\rightarrow$ FAQ0136.

- 2. In "Port" option, choose "SW", and then tick "SWJ" option;
- 3. Confirm that the "ARM SW-DP" is recognized.



Cortex-M Target Driver Setup		×
Debug   Trace   Flash Downlo	<sup>a</sup> ] <b>3</b>	1
CMSIS-DAP - JTAG/SW Adapte	- SW Device	
AT-Link (WinUSB) CMSIS-DA	IDCODE Device Name	Move
Any	SWDIO SWDIO SW0BC11477 ARM CoreSight SW-DP	Up
AT-Link (WinUSB) CMSIS-DAP Firmware Version; [2, 1, 2		Down
2 SWJ Port: SW -	Automatic Detection ID CODE:	
Max Clock: 5MHz	C Manual Configuration Device Name:	
	Add Delete Update	AP: 0x00

Then, click "Utilities"  $\rightarrow$  untick "Use Debug Driver" (the red box marked 1)  $\rightarrow$  select "CMSIS-DAP Debugger" (the red box marked 2)  $\rightarrow$  finally tick "Use Debug Driver" (note: users need to untick this box first and then tick it).

Figure 13. Keil Utilities option

Device   Target   Output   Listing   User	C/C++ Asm Linker Debug Vtilities	
Configure Flash Menu Command • Use Target Driver for Flash Programming	1 Use Debug Driver	
	Settings Update Target before Debugging	
Init File:	Edit	

If AT-Link is to be used in IAR environment, click "Project"  $\rightarrow$  choose "Options"  $\rightarrow$  go to "Debugger" and choose "CMSIS-DAP"  $\rightarrow$  tick "SWD".

1 🖻 🖬 🗿	C	Add Files	- < (	२ > ⇆ म्ह < 📮	> < > • • • • • • • • • • • • • • • • •
kspace		Add Group			
ua	[±]	Import File List			
		Add Project Connection			
template		Edit Configurations	та	Options for node "tem	molate" X
e sp envir	×	Remove	ion v2		•
E firmware	to	Create New Project	20 f ma		
🗄 🛋 readme	ž	Add Existing Project	*****	Category:	Factory Settings
🗐 🛋 user	~			General Options	
-⊞ [] at32f4	٥	Options Alt+F7	oftware	Static Analysis	
-⊞ © at32140		Version Control System	load fro	Runtime Checking C/C++ Compiler	Setup Download Images Extra Options Multicore Plugins
🗄 📕 Output	0	Make F7	are and	Assembler	
		Compile Ctrl+F7	lopment	Custom Build	Driver 🗹 Run to
		Rebuild All	are is	Build Actions	CMSIS DAR
	1	Clean	SOFTWAR	Linker	Simulator
		Batch build F8	NTEES O	Simulator	CADI
	-		TOPY OF	CADI	CMSIS DAP
		C-STAT Static Analysis	DING BU	CMSIS DAP	GDB Server
	8	Stop Build Ctrl+Break	SS FOR .	I-jet/JTAGjet	J-jet/JTAGjet
	O	Download and Debug Ctrl+D		J-Link/J-Trace	TI Stellaris
		Debug without Downloading		Nu-Link	Nu-Link
	$\mathbf{\hat{b}}$	Attach to Running Target	"at.32f4	PE micro	ST-LINK
	G	Make & Restart Debugger Ctrl+R	"at32f4	ST-LINK Third-Party Driver	Third-Party Driver
	c	Restart Debugger Ctrl+Shift+R		TI MSP-FET	TI MSP-FET
		Download +	.ogroup .	TI XDS	hdebugger\ArteryTek\A132F40/xG
		SFR Setup			
		CMSIS-Manager	ogroup		
		Open Device Description File			
		Save List of Pergisters			OK Cancel

Figure 14. IAR Debug option

Figure 15. IAR CMSIS-DAP option

General Options	1			
Static Analysis				
Runtime Checking				
C/C++ Compiler	Setup	Interface	Breakpoints	
Assembler	Droho	confin	Probe configuration file	
Output Converter	Probe	comig	Trobe configuration file	
Custom Build	Au	to	Override default	
Build Actions	0.11			
Linker	O Fro	om file		
Simulator			CDU	Calaat
CADI		plicit		Select
CMSIS DAP	Interfe	~~	- Evolicit probe configure	ation
GDB Server	interia	ice	Explicit probe conligura	ation
I-jet/JTAGjet		AG	Multi-target debug	system
J-Link/J-Trace	0111	-	Tanat and a CAR	n an Markida an O
TI Stellaris	© SW	/D	Target number (TAF	or Wultidrop
Nu-Link			Target with multi	nle CPUs
PE micro				
ST-LINK			CPU number or	n <b>0</b>
Third-Party Driver	Interface	•		
		-		
11 ADS	Auto d	etect 🗸 🗸		

Note: The document "AT32F425firmware\_BSP&Pack\_user\_guide" provides details on Flash algorithms, MCU product series replacement and J-Link. This document is available from <u>ARTERY official website</u>  $\rightarrow$  Products $\rightarrow$  Value line $\rightarrow$ AT32F425 series $\rightarrow$ BSP (download and unzip, and then go to "VAT32F425\_Firmware\_Library\_Vx.x.x\document").

## 1.1.4 How to quickly replace AT32F415 with AT32F425

- The migration guide from AT32F415 to AT32F425 is detailed in the document *"MG0019\_Migrating from AT32F415 to AT32F425"*, which is available from ARTERY official website → Product → Value line → AT32F425 series page.
- If program failure occurs, please refer to the corresponding sections of this document, or you can contact the agent and Artery's technical staff for support.

Note: For more information on how to get better AT32F425 operating performance, refer to the application note "AN0004\_Performance\_Optimization" from ARTERY official website  $\rightarrow$  Product  $\rightarrow$  AP Note  $\rightarrow$  AN0004.

## **1.2** AT32F425 functionality configuration

## **1.2.1** Instruction prefetch buffer

Instruction prefetch buffer helps to achieve quicker CPU execution speed. After instruction prefetch buffer is enabled, the subsequent word is already awaiting in the buffer while CPU is reading the current word. The instruction prefetch controller will then determine whether or not to access Flash memory according to available space in the buffer. If there is at least a free space in the instruction prefetch controller will perform a read access.

Different system clocks require different wait states, which can be set through the bit [2:0] (WTCYC) in the FLASH\_PSR register.



Bit	Abbr.	Reset value	Туре	Description
Bit 2:0	WTCYC	0x0	rw	Wait states The wait states depends on the size of the system clock and they are in terms of system clocks. 0: Zero wait state 1: One wait state 2: Two wait states 3: Three wait states The system clock sets the wait state on a 32-MHz basis: Zero wait state for the first 32 MHz One wait state for the second 32 MHz Two wait states on the third 32 MHz Three wait states on the fourth 32 MHz

#### Figure 16. Wait state bit in FLASH\_PSR register

AT32 library has made relevant settings in the "system\_clock\_config()" function. For BSP of other AT32 MCU series, you can also find this settings at the same location.

Figure 17. system\_clock\_config function

i i i i i i i i i i i i i i i i i i i	void system_clock_config(void)
	<pre>/* config flash psr register */ flash_psr_set(FLASH_WAIT_CYCLE_2);</pre>
	/* reset crm */ crm_reset();
	crm_clock_source_enable(CRM_CLOCK_SOURCE_HEXT, TRUE);
	<pre>/* wait till hext is ready */ while(crm_hext_stable_wait() == ERROR) { }</pre>

## 1.2.2 PLL clock configuration

AT32F425 embeds a PLL with a maximum of 96 MHz clock output. The AT32F425 PLL clock can be configured by setting the CRM\_CFG or CRM\_PLL register. The CRM\_PLL register can be used to configure different PLL clock frequencies, with the following formula:

PLL output clock = PLL reference input clock × PLL frequency multiplication factor PLL\_NS PLL predivider factor (PLL\_MS) × PLL post – divider factor (PLL\_FR)

Example of PLL settings using CRM\_CFG register, based on HEXT=8MHz, PLL=96MHz

crm\_pll\_config(CRM\_PLL\_SOURCE\_HEXT, CRM\_PLL\_MULT\_12);

Example of PLL settings using CRM\_PLL register, based on HEXT=8MHz, PLL=94MHz

 Figure 18. AT32F425 94MHz output clock

 #define CRM\_PLL\_NS ((uint16\_t)0x2F) /\* PLL\_NS=47 \*/

 #define CRM\_PLL\_MS ((uint16\_t)0x01) /\* PLL\_MS=1 \*/

 /\* config pll clock resource PLL\_FR =4\*/

 crm\_pll\_config2(CRM\_PLL\_SOURCE\_HEXT, CRM\_PLL\_NS, CRM\_PLL\_MS, CRM\_PLL\_FR\_4);



Where, the "CRM\_PLL\_SOURCE\_HEXT" parameter indicates that the HEXT is used as an external clock source, PLL\_NS=47, PLL\_MS=1, and PLL\_FR value is "CRM\_PLL\_FR\_4 (0x02, divided by 4)".

For details about clock configuration, please refer to  $AN0121\_AT32F425\_CRM\_Start\_Guide$ . This document is available from ATERTY official website  $\rightarrow$  Support  $\rightarrow$  AP Note  $\rightarrow$  AN0121. It introduces how to configure and modify AT32F425 clock source, and how to use the New Clock Configuration tool to quickly generate the desired clock code and apply it to projects.

## 1.2.3 Encryption

Note: The BOOT1 bit of AT32F425 series is located in the user system data area (0x1FFF F800). When ISP tool is used, it is mandatory to ensure that nBOOT1=1 is asserted (default value) so that the program is booted from system memory instead of SRAM.

### **1.2.3.1 Access protection**

Access protection is commonly referred to as "encryption" and applies to the entire Flash memory. Once the Flash access protection is enabled, the internal Flash memory can only be read through normal execution of the program, instead of through JTAG or SWD. Using ISP or ICP tool to unlock access protection will trigger erase operation to the Flash memory.

# Note: The high-level access protection, after being enabled, cannot be unlocked. Meanwhile, it is forbidden for users to erase and write system data area in any way.

Users can use ICP/ISP programmer to enable or disable access protection.

■ Artery ICP Programmer (BOOT0=0)

Enable access protection: Target – Access protection – Enable access protection or enable high-level access protection (see Figure 19 below).

Unlock access protection: Target – Access protection – Disable

🐻 Artery ICP P	rogrammer_V3.	.0.02		- 🗆 🗙
File J-Link	settings AT-	Link settings	Target Language Help	
Disconnect	Part Number	r: AT32F425F	Mass erase Frase main flash	
AT-Link Y	AT-Link-EZ AT-Link SN:	FW: V2.1.0 7369593300C0	Erase sectors	雅 持 力
	SPIM	FLASH DA	User system data	
	Type	-	Access protection	<ul> <li>Enable access protection</li> </ul>
Memory read	settings		sLib status	Enable high level access protection
Address 0x	08000000	Read size Ox	Boot memory AP mode	Disable Read

#### Figure 19. Use ICP tool to enable/disable access protection

■ Artery ISP Programmer (BOOT0=1)

Enable access protection: Keep clicking "Next" until you enter the final interface. Then tick "Protection" -- choose "Enable" and "Access protection" -- click "Yes" (see Figure 20 below). Unlock access protection: Tick "Protection" -- choose "Disable" and "Access protection" -- click "Yes".

■ Artery ISP Multi-Port Programmer (BOOT0=1)

Enable access protection: Tick "Protection" -- choose "Enable" and "Access protection" or "High-level access protection" -- click "Start".



Unlock access protection: Tick "Protection" -- choose "Disable" and "Access protection" -- click "Start".

👞 Artery I	ISP Programmer_V2.0.03		- 🗆 X
	#17F=7	Y雅特	力
⊖ Erase	All O Sectors	x = x	🔵 Edit User system data
O Downlo	oad to device		🔿 Disable sLib
sLib	Status: DISABLE	Start sector	$\sim$
		INSTR start sector	
Passy	word Ox	End sector	$\sim$
No	File Name	File Size Address Ba	nge(Ox) Add
1	425. hex	3652 08000000-0	8000E43 Delete
	Carfing		
۲	Comirm		^ >
Erase	e option		e download
✓ 0p	ptimize(B 🕐 Are you su	re to enable the access protection	on? load
Wr	rite user	3	brogram
Addr	ress Ox		× 00000001
Ap	pply User	A2(1)	
🗹 En	nable Access protection after	Download Access protection	· ~
	d from device		
0 0 0 1 0 0 0			
O Firmwa	are CRC Sector fill	FF	
○ Flash	CRC		
1	Start sector Sector0-0x800	DODOO v End sector Sec	tor0-0x8000000 ~
• Protec	ction ENABLE ~ Acc	ess protection	✓
		2 Next	Close
		-	

#### Figure 20. Use ISP to enable access protection

#### Figure 21. Use ISP to disable access protection

Artery		雅特ノ	- • ×	
C Erase	All O Sectors	O Edi	t Vser system data	
	Statur: DISARIE	O Dis	able sLib	
	Status, Storman	INSTR start sector		
Pars	word Ox	End sector	$\sim$	
<b>No.</b> 1	File Name 425. hex	File Size Address Range(0x) 3652 0800000-08000E43	Add	
	you sure to disable the acc	ass erased and all contents will be i	ost Are	
A V E	able Access protection after Dow	nload Access protection	香(N)	
A Uploa	able Access protection after Dow	nload Access protection	蒼(1)	
Uploa Firms	able Access protection after Dev 1 from device ure CRC Sector fill F	nload Access protection	<b>蒼(N)</b>	
Uplos Firms Flash	able Access protection after Dev from device re CRC Sector fill F	nload Access protection	蒼(N)	
Uploa Firms Flash	able Access protection after Dow 1 from device re CBC Sector fill F CBC Start sector Sector0-0x800000	ses protection?	音(N)	

Note: Access protection, after being enabled, cannot be unlocked through erase operation.



## 1.2.3.2 Erase/program protection

Write protection applies to the entire Flash memory or to part of Flash area. Once the Flash write protection is enabled, the internal Flash cannot be written.

Users can use ICP/ISP programmer to enable or disable erase/program protection.

Artery ICP Programmer (BOOT0=0)
 Enable erase/program protection: Target – User system data – tick the page to be erase/program-protected – Apply to device.
 Disable erase/program protection: Target – User system data – untick the page to be

erase/program-protected – Apply to device.

Artery ISP Programmer (BOOT0=1)

Enable erase/program protection: Are you sure to enable erase/program protection?--Yes. Disable erase/program protection: Are you sure to disable erase/program protection?--Yes.

■ Artery ISP Multi-Port Programmer (BOOT0=1)

Enable erase/program protection: Are you sure to enable erase/program protection?--Yes. Disable erase/program protection: Are you sure to disable erase/program protection?--Yes.

											~
FAP A5 Dis	able			~							
-System setting byt					ост	CT	DRV D	ст		ROOTI	
SSB FF	nWDT_DEP	SLP	⊘ nW	IDT_STD	BY	V 1131	001_K	31	M	100011	
Erase and program	m protectio	on by	tes								
Name	Start addres	ss E	ind addres	is Size	e	EPP	^	EPP0-3	[	FD FF FF FF	]
Sector3	0x8000C00	0	x8000FFF	0x4	400(1K)	N					
Sector4	0x8001000	0	0x80013FF	0x4	100(1K)	Y	_				
Sectors	0x8001800	0	v80018EE	0v4	100(1K)	v					
Sector7	0x8001C00	0	x8001FFF	0x4	100(1K)	Y					
Sector8	0x8002000	0	x80023FF	0x4	400(1K)	N					
Sector9	0x8002400	0	x80027FF	0x4	400(1K)	N	~	Sel	ect a	I	
User data											
Date	0	1	2	3	4	5	6	7	^	Clear	
Data 07 (0x)	FF	FF	FF	FF	FF	FF	FF	FF			
Data 815 (0x)	FF	FF	FF	FF	FF	FF	FF	FF			
Data 1623 (0x)	FF	FF	FF	FF	FF	FF	FF	FF		Load file	
Data 2431 (0x)	FF	FF	FF	FF	FF	FF	FF	FF	~	Save to file	
Data 2431 (0x)	FF	FF	FF	FF	FF	FF	FF	FF	~	Save to file	

#### Figure 22. Use ICP tool to enable erase/program protection

											-	
🐻 Artery I	CP Programme	r_V3.0.02	2									$\times$
Eile	ink settinas	AT-Lin	k settir	nas	Target	Lan	quade	He	In			
🐻 User	system data											$\times$
Access	protection											
FAP	A5 Disable	•			~							
System	setting byte											
	- V nV	VDT ATO	EN	nDE	PSLP R	ST	nST	DBY RS	т		BOOT1	
SSB F	F G	-	-		-			-				
	⊡ nv	VD1_DEP:	SLP	⊵ nw	DI_SIDE	SY						
Erase	and program p	protectio	on byte	s					_			
Name	e Sta	art addres	ss End	l addres	s Size		EPP	> ^	EPP0-3	ſ	FF FF FF FF	
🗆 Se	ctor3 0x	8000C00	0x8	000FFF	0x40	00(1K)	N			L		
Se Se	ctor4 0x	8001000	0x8	0013FF	0x40	00(1K)	N					
Se Se	ctor5 0x	8001400	0x8	0017FF	0x40	00(1K)	N					
Se Se	ctor6 0x	8001800	0x8	001BFF	0x40	00(1K)	N					
Se Se	ctor7 0x	8001C00	0x8	001FFF	0x40	00(1K)	N					
Se Se	ctor8 0x	8002000	0x8	0023FF	0x40	00(1K)	N					
Se Se	ctor9 0x	8002400	0x8	0027FF	0x40	00(1K)	N	~	Sele	ect al	I	
User d	ata											
Date		0	1	2	3	4	5	6	7	^	Clear	
Data (	)7 (0x)	FF	FF	FF	FF	FF	FF	FF	FF			
Data 8	815 (0x)	FF	FF	FF	FF	FF	FF	FF	FF			
Data	623 (0x)	FF	FF	FF	FF	FF	FF	FF	FF		Load file	
Data	2431 (0x)	FF	FF	FF	FF	FF	FF	FF	FF	~	Save to file	
	Load from	n device	A	pply to	device		Load f	rom file	e	S	ave to file	
												¥

Figure 23. Use ICP tool to disable erase/program protection

Note: Erase/program protection, after being enabled, cannot be unlocked through erase operation.

### 1.2.4 Set system memory as main memory extension

System memory is used as a boot mode by default to store microcontroller manufacturer' Startup Code. On top of this, in AT32F425 series, a new feature is added to the system memory by using it to store user-defined codes as an extended memory area (AP mode).

# *Note:* System memory AP mode is irreversible and can only be set once, meaning that after AP mode is selected, its original BOOT mode cannot be resumed.

During product development, users can use Artery ICP Programmer to enable system memory as an extended memory according to the following procedures.

- Connect AT-Link or J-Link to AT-START-F425 board and supply power;
- Open Artery ICP programmer and choose AT-Link or J-Link connection;
- Go to menu bar: Target Boot memory AP mode OK.

F* Artery ICP Programmer_V3.0.02       - · · · ×         File       J-Link settings       AT-Link settings       Target       Language       Help         Disconnect       Part Number:       AT32F425       Mass erase       Frase main flash         AT-Link       EX       FW: V2.10       Mass erase       Frase main flash         AT-Link       EX       FW: V2.10       AT-Link SN: 7369593300C       User system data         IT-Link       SPIM       FLASH_D       Access protection       11/PA12 pins)         Type       3       Boot memory AP mode       Read         Memory read settings       Boot memory AP mode       Read         File info       DownLoad       Flash info       Marming         Files info       Varming       X       Address ran;       DownLoad         Flash info       Warming       X       Innecoverable after setting;       00 00 00 00 00 00 00 00 00 00 00 00 00				
File       J-Link settings       AT-Link settings       Target       Language       Help         Disconnect       Part Number:       AT32F4255       Mass erase       Erase main flash         AT-Link       AT-Link SR:       7365933300C       User system data       ATCPET         AT-Link       SPIM       FLASH_D       User system data       ACcess protection       I/PA12 pins)         Memory read settings       Address 0x       08000000       Read size       Boot memory AP mode       Read         File info       DownLoad       Flash CRC       Oxl       Add         Opration Progress       Enabling AP mode       Debug       Delete         Address rang       AP Mode can only be set once, and the data of boot memory is uncerverable after setting.       DownLoad         Matterss       AP Mode can only be set once, and the data of boot memory is uncerverable after setting.       Do do ac         0x0800000       AP Mode can only be set once, and the data of boot memory is uncerverable after setting.       Do do ac         0x0800000       AP Mode can only be set once, and the data of boot memory is uncerverable after setting.       Do do ac         0x0800000       AP Mode can only be set once and the data of boot memory is uncerverable after setting.       Do do ac         0x0800000       Or ut uv uo or ut uv uo or ut uv	10 Artery ICP	Programmer_V3.0.02 2		- 🗆 X
Disconnect       Part Number:       AT32F425i         AT-Link       AT-Link SN:       7369593300ct         AT-Link       SPIM       FLASH DA         Type       SPIM       FLASH DA         Type       Solution       Solution         Address       0x 8000000       Read size 0x         Boot memory AP mode       Read         DownLoad       Flash CRC       (0x)         Opration Progress       Debug       DElete         Opration Progress       Delete       Delete         Address rant       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         Address rant       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         Address rant       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         Nox8000000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         Nox800001       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         Nox8000000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         Nox8000001       AP Mode can only be set once and the dat	1 File J-Link	settings AT-Link settings	Target Language Help	_
AT-Link       AT-Link SN: 7369593300C         SPIM       FLASH DA         Type       User system data         Access protection       0/PB11 pins)         SLib status       Boot memory AP mode         Read       DownLoad         File info       DownLoad         I 425.hex       Debug         Opration Progress       Enabling AP mode         Enabling AP mode       No.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.         Address rang       AP Mode can only be set once, and the data o	Disconnect	Part Number: AT32F425F	Mass erase Frase main flash	
Ver Luik       SPIM       FLASH Dr         Type       SPIM       FLASH Dr         Type       SPIM       SPIM         Address       0x0800000       Read         DownLoad       Flash CRC       (0x)         Opration Progress       Debug       Delete         Opration Progress       Debug       DownLoad         Flash info       Warning       X         Address ran;       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       DownLoad         No.8000000       Address ran;       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       Do 88.7.1         Ox08000000       or us wo	AT-Link v	AT-Link-EZ FW: V2.1.0 AT-Link SN: 7369593300C0	Erase sectors	雅结力
Type       Access protection       O/PB11 pins)         Address 0x 08000000       Read size 0x       Boot memory AP mode       Read         File info       DownLoad       Filsh CRC       (0x)       Add         No.       File name       Debug       DeEdd       Delete         Opration Progress       Enabling AP mode       CovenLoad       DevenLoad         Flash info       Warning       Address rans       DownLoad         Address rans       AP Mode can only be set once, and the data of boot memory is       0 08 2.1         Ox8000000       AP Mode can only be set once, and the data of boot memory is       0 08 2.1         Ox8000000       AP mode can only be set once, and the data of boot memory is       0 08 2.1         Ox8000000       AP mode can only be set once, and the data of boot memory is       0 08 2.1         Ox8000000       AP mode can only be set once, and the data of boot memory is       0 08 2.1         Ox8000000       AP mode can only be set once, and the data of boot memory is       0 08 2.1         Ox8000000       AP mode can only be set once, and the data of boot memory is       0 08 8.2         Ox80000000       AP mode can only be set once, and the data of boot memory is       0 08 8.2         Ox80000000       AP mode can only be set once, and the data of boot memory is       0 08 8.		SPIM FLASH_DA	User system data	11/PA12 pins)
Memory read settings       SLib status         Address 0x       08000000       Read size       0x         Boot memory AP mode       Read         File info       DownLoad         File info       DownLoad         I       425.hex       Debug       00E43         Opration Progress       Enabling AP mode       DownLoad         Flash info       Warning       Address rans         Address rans       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       08         0x0800000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       0         0x0800000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       0         0x0800000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       0         0x0800000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       0         0x0800000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       0         0x08000000       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       0       0         0x08000000 <th></th> <th>Туре</th> <th>Access protection</th> <th>10/PB11 pins)</th>		Туре	Access protection	10/PB11 pins)
Address 0x       08000000       Read size 0x       Boot memory AP mode       Read         File info       DownLoad       Flash CRC       (0x)       Add         1       425.hex       Debug       0E43       Delete         Opration Progress       Enabling AP mode       DownLoad         Flash info       Marring       X         Address rans       AP Mode can only be set once, and the data of boot memory is       0       <	Memory rea	d settings 3	sLib status	
File info     DownLoad       I     425.hex       Opration Progress       Enabling AP mode       Enabling AP mode       Address rans       Address	Address 0x	08000000 Read size 0x	Boot memory AP mode	Read
No.       File name       Flash CRC       (0x)       Add         1       425.hex       Debug       0E43       Delete         Opration Progress       Enabling AP mode       DownLoad         Flash info       Warning       X         Address rans       AP Mode can only be set once, and the data of boot memory is on 08 ?.r       00 88 ?.r         0x08000000       0x08000010       0x08000010       0x08000010         0x08000010       0r       0r       0r       0r         0x08000010       0r       0r       0r       0r       0r         0x08000010       0r       0r       0r       00 08 ?.r       00 08 ?.r         0x08000010       0r       0r       0r       0r       0r       0r       0r         0x08000010       0r       r	File info		DownLoad	
1     425.hex     Debug     00E43     Delete       Opration Progress     Enabling AP mode     DownLoad       Flash info     Warning     X       Address ran;     Address ran;     Image: Comparison of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 000000     Image: Comparison of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 000000     Image: Comparison of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 00 00     Image: Comparison of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 00 00     Image: Comparison of the set once, and the data of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 00 00     Image: Comparison of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 00 00     Image: Comparison of the set once, and the data of the set once, and the data of boot memory is 00 88 ?.r     00 88 ?.r       00 00 00     Image: Comparison of the set once, and the data of the set once, and the data of the set once, and	No. File	name	Flash CRC	(0x) Add
Opration Progress         Enabling AP mode       DownLoad         Flash info       Warning         Address ran;       Address ran;         Address ran;       AP Mode can only be set once, and the data of boot memory is 00 88 ?. r         Ox8000000       AP Mode can only be set once, and the data of boot memory is 00 88 ?. r         Ox8000000       AP Mode can only be set once, and the data of boot memory is 00 88 ?. r         Ox8000000       AP Mode can only be set once, and the data of boot memory is 00 88 ?. r         Ox8000000       AP Mode can only be set once, and the data of boot memory is 00 88 ?. r         Ox8000000       AP Mode can only be set once, and the data of boot memory is 00 88 ?. r         DownLoad       E F At 00 08 m         Ox8000000       AP Mode can only be set once, and the data of boot memory is 00 08 m         DownLoad       E F At 00 08 m         DownLoad       E F At 00 08 m         DownLoad       E F At 00 08 m         DownBoot 00 08 m       DownLoad         DownLoad       E F At 00 08 m	1 425	hex	Debug	00E43 Delete
Address ran;       Address ran;       Address ran;       Address ran;       Address ran;       E F Ad A         Address ran;       AP Mode can only be set once, and the data of boot memory is unrecoverable after setting.       00 08 2; r         0x08000000       0x08000000       00 08 2; r         0x08000020       00 08 2; r         0x08000030       00 08 2; r         0x08000040       00 08 2; r         0x0800040       00 08 2; r         0x08005; r       00 08 2; r <td< th=""><th>Flash info</th><th>Opration Progress Enabling AP mode Warning</th><th></th><th>DownLoad</th></td<>	Flash info	Opration Progress Enabling AP mode Warning		DownLoad
下午 02:45:00 : Target device connection successfully!	Address fairs 0x08000000 0x08000010 0x08000020 0x08000030 0x08000040	AP Mode can only be set unrecoverable after settin	conce, and the data of boot memory is ng.	E         F         A!           00         08         ?. r           00         00         00           00         00         00           00         08            00         08         2           00         08         2           00         08         2           00         08         2
	下午 02:45:00 :	Target device connection successfull	jy!	^

Figure 24. Use ICP tool to set boot memory AP mode

To avoid unexpected wrong operations, users need manually enter the passkey "0xA35F6D24, and then check whether the operation is successful or not in "File info".

Artery ICP	Programmer V3.0.02 — — X
File J-Link	settings AT-Link settings Target Language Help
Disconnect	Part Number: AT32F425R8T7-7 FlashSize: 64KB
AT-Link ~	AT-Link-EZ FW: V2.1.0 AT-Link SN: 7369593300C0636C0A17E102 (WinUSB) 雅特力
Add Enable	SPIM     FLASH_DA 0x     0 <ul> <li>Remap0 (Use PA11/PA12 pins)</li> <li>mode enable key</li> <li>-</li> <li>×</li> <li>key:(0x)</li> <li>(0xA35F6D24)</li> <li>OK</li> <li>Cancel</li> <li>Address range(0x)</li> <li>Delete</li> <li>OB00000-08000E43</li> <li>Delete</li> <li>on Progress</li> <li>ng AP mode</li> <li>rerify</li> <li>DownLoad</li> <li>le:425.hex</li> </ul>

Figure 25. Boot memory AP mode operating progress

In mass production stage, users can use Artery ICP Programmer to enable system memory as memory extension area according to the following procedures:

Connect AT-Link to AT-START-F425 board and supply power;

Note: The onboard AT-Link EZ edition of AT-START-F425 does not support offline programming. Therefore, users can only use other editions.

• Open Artery ICP programmer and choose AT-Link connection;



- Go to menu bar: AT-Link setting -- AT-Link offline configuration setting;
- Follow the steps below to generate off-line project:
  - 1. Click "Create"
  - 2. Enter the project name
  - 3. Select a the desired MCU series and MCU part number
  - 4. Add *.hex* file
  - 5. Choose SWD as download interface
  - 6. Tick "Boot mode AP mode" option and enter the passkey
  - 7. Save project file or save project to AT-Link

In addition to above settings, users can also make other configurations as needed.

nk settings AT-Link offline config settings AT-Link offline download status ine project Delete 3 ect name test1 Device AT32F425 AT32 . File name File size Address range(0x) Str run_in_boot_memory.hex 3800 08000000-08000ED7 run_in_boot_memory.hex 68 1FFFE400-1FFFE443	2F425R8T7-7 v orage locad Add
ine project Bevice AT32F425 V AT32 File name test1 File size Address range(0x) State run_in_boot_memory.hex 3800 08000000-08000ED7 run_in_boot_memory.hex 68 1FFFE400-1FFFE443 Delete	2F425R8T7-7 orage loca
Bert name     test1       Device     AT32F425       AT32F425     AT32       File name     File size       run_in_boot_memory.hex     3800       08000000-08000ED7       run_in_boot_memory.hex     68	2F425R8T7-7 orage loca
ect name     test1     Device     AT32F425     AT32       .     File name     File size     Address range(0x)     Str       run_in_boot_memory.hex     3800     08000000-08000ED7       run_in_boot_memory.hex     68     1FFFE400-1FFFE443	2F425R8T7-7
. File name File size Address range(0x) Str run_in_boot_memory.hex 3800 08000000-08000ED7 run_in_boot_memory.hex 68 1FFFE400-1FFFE443	orage loca
run_in_boot_memory.hex         3800         0800000-08000ED7           run_in_boot_memory.hex         68         1FFFE400-1FFFE443	4 Delete
run_in_boot_memory.hex 68 1FFFE400-1FFFE443	001000
	>
se option Erase the sectors of file size $\lor$	
Reset and run	
Access protection	e
Key:(ux) A35F6D24	(0xA35F6D2
Tware serial number(SN) SPIM settings sLib settings	
Write software serial number	
Write address in flash: 0x 08010000	
nitial SN: 0x 00000001	
ncrease step: 0x 00000001	
Load parameters	Course and an and an a
	save parameters

In Step 7, if you choose "Save project file", the project will be saved as .atcp file so that it can be loaded onto other AT-Link.

The following dialogue window will pop out during actual operation. If "This project is only used at the specified AT-Link" option is ticked, it means that this project is bonded to a particular AT-Link and can only be used in this AT-Link. In this case, users need to enter AT-Link serial number which will be bonded to. If "This project is only used once" option is ticked, it means that this project could only be used once in the same AT-Link.

 . <u></u>				5
₩ AT-Link project file s	settings	-		×
This project is or	nly used at the specified A	AT-Link.		1
AT-Link SN:	88A150320000B32905	177402		
This project is or	ily used once.			
AT-Link AIN:	07318178B80B910B			
	0	К	Cancel	1

Figure 27. Use ICP tool to set offline project programming

In step 7, if you choose "Save project to AT-Link" and operation is successful, in "AT-Link offline download status" option, you need to choose a project name for offline download; click "Save and activate", and then click "Start download".

#### Figure 28. ICP tool to monitor offline download status

G AT-Link Setting			-		×
AT-Link settings AT-Link offline c	config settings AT-Lin	k offline download status			
Select offline download item: test	Save and activate	Download interface: ISP uart baud rate: ISP boot mode:	SWD 115200 AutoM	) atic	~
Activated project: test Total downloads: Unlimited Downloaded times: 2	Succes	sful downloads: 2			
File download successfully! !	!	Start	downloa	ad	
		Start buttor Cancel butto	n <b>free d</b> a	ownload Iownloa	d

- For more information on system memory extension, please refer to the document AN0066\_config\_boot\_memory\_as\_extension\_of\_main\_memory(AP\_mode), which is available from ARTERY official website → Support → AP Note → AN0066.
- For demos running user program in the system memory, please refer to the BSP, which is available from ARTERY official website → Product → Value line → AT32F425 series → BSP (download and unzip, and then go to "AT32F425\_Firmware\_Library\_V2.x.x\utilities\at32f425\_boot\_memory\_ap\_demo")



## 1.2.5 How to distinguish AT32 MCU from other MCUs

Read Cortex-M series CPU ID number to determine whether it is based M0, M3 or M4 core.

```
Figure 29. Read Cortex ID

cortex_id = *(uint32_t*)0xE000ED00;// read Cortex ID

if((cortex_id == 0x410FC240) || (cortex_id == 0x410FC241))

{

printf("This chip is Cortex-M4F.\r\n");

}

else

{

printf("This chip is Other Device.\r\n");

}
```

#### Read PID and UID

/\* Get AT32 MCU PID/UID base address \*/ #define DEVICE\_ID\_ADDR1 0x1FFFF7F3 // define MCU device ID and UID base address #define DEVICE\_ID\_ADDR2 0xE0042000 // define MCU device ID and PID base address /\* store ID \*/ uint8\_t  $ID[5] = \{0\};$ /\* AT32F425 MCU type table \*/ constuint64\_tAT32\_MCU\_ID\_TABLE[] = { 0x0000010050092100, //AT32F425R8T7 64KB LQFP64 0x0000010050092081, //AT32F425R6T7 64KB LQFP64 }; /\* get UID/PID \*/ ID[0] = \*(int\*)DEVICE\_ID\_ADDR1;  $ID[1] = *(int^*)(DEVICE_ID_ADDR2+3);$ ID[2] = \*(int\*)(DEVICE\_ID\_ADDR2+2); ID[3] = \*(int\*)(DEVICE\_ID\_ADDR2+1);  $ID[4] = *(int^*)(DEVICE_ID_ADDR2+0);$ /\* combine UID/PID \*/ AT\_device\_id = ((uint64\_t)ID[0]<<32)|((uint64\_t)ID[1]<<24)|((uint64\_t)ID[2]<<16)|((uint64\_t)ID[3]<<8)|((uint64\_t)ID[4]<<0); /\* identify AT32 MCU \*/ for(i=0;i<sizeof(AT32\_MCU\_ID\_TABLE)/sizeof(AT32\_MCU\_ID\_TABLE[0]);i++) if(AT\_device\_id == AT32\_MCU\_ID\_TABLE[i]) { printf("This chip is AT32F4xx.\r\n"); } else { printf("This chip is Other Device.\r\n"); }

#### Figure 30. Read PID and UID



Note: AT32F4xx MCU contains several ID codes. By organizing the obtained ID information into a 64-bit data, it is possible for users to determine which MCU series is being used. For details, refer to the "Debug" section of the corresponding reference manual and *AN0016\_Recognize\_AT32\_MCU*.

## 2 FAQs about download and compiling

## 2.1 Program enters Hard Fault Handler

Access data outside its boundary limit

Locate where the program exceeds the boundary, and move it to normal data area.

- The SRAM used by the program is outside the programmed MCU SRAM threshold.
- System clock is set out of specification.

## 2.2 JLink unable to recognize IC in Keil project

For a possible solution, please refer to the following documents:

- *"FAQ0008\_J-Link\_cannot\_find\_IC"*, which is available from ARTERY official website →Support→FAQ→FAQ0008.
- *"FAQ0132\_How\_to\_add\_Artery\_MCU\_into\_JLINK*", which is available from ARTERY official website → Support → FAQ → FAQ0132.

## 2.3 Errors during download

## 2.3.1 Flash Download failed–"Cortex-M4"

A warning message pops up during Keil debugging or downloading:



38 Timing µVision
40 while(
41 } 42 - Frror: Elash Download failed - "Cortex-M4"
43 p/**
44 * @bri
45 * Cpar
47 47 47 47 47 47 47 47 47 47 47 47 47 4
48 void Tim
49 🗉 {

The warning message pops up in one of the following conditions:

- Access protection is enabled. Disable MCU access protection before download.
- An incorrect Flash algorithm file is selected or Flash algorithm file is not loaded. Select and add the correct Flash algorithm to "Flash Download".
- Wrong BOOT0 setting. The BOOT0 must be set to 0 to boot MCU from main Flash memory.
- J-Link driver version is incorrect. Versions 6.20C and above are recommended.
- JTAG/SWD PIN disabled. Refer to Section 2.2.5 for solution.



### 2.3.2 No Debug Unit Device found

- Download interface is being occupied. For example, ICP is being connected to a target device.
- JTAG/SWD connection error or it is not connected.

## 2.3.3 RDDI-DAP Error

- The compiler optimization level is too high. For example, Keil AC6 optimization level is the default "-Oz", which should be changed to "-O0/-O1".
- JTAG/SWD PIN disabled. Refer to Section 2.2.5 for solution.

## 2.3.4 ISP serial interface gets stuck during download

When the ISP serial interface is used for download, it may get stuck so that it cannot be released. It is recommended to:

- Check if the power supply is stable
- Use a better USB-to-serial interface tool, such as CH340 chip.

## 2.3.5 How to resume program download

Users may not be able to download programs in one of the following conditions:

- JTAG/SWD PIN disabled, so that program download failed and the JTAG/SWD device cannot be found.
- Entered Standby mode Standby mode, so that program download failed and the JTAG/SWD device cannot be found.

The following solutions are recommended:

- Solution 1: Switch boot mode Switch boot mode to Boot0=1, and then press "Reset" button to resume download (note to return to Boot0=0 after download resumes). This method also applies to ISP download.
- Solution 2: Use ICP tool to add AT-Link The AT-Link is specially designed for AT32 MCUs; therefore, it is possible to resume download by adding AT-Link through ICP tool.



## 3 Security Library (sLib)

## 3.1 Introduction

As more and more MCU applications require complex algorithms and middleware solutions, it has become an important issue that how to protect IP-Codes (such as core algorithms) developed by software solution providers.

In response to this demand, the AT32F425 series is designed with a security library (sLib) to protect important IP-Codes against being changed or read by the end user program.

## 3.2 Application principles

- Security library (sLib) is a defined area protected by a code in the main memory. Software solution providers store core algorithms in sLib for protection. The rest of the area can be used for secondary development by end users.
- Security library includes the read-only area (SLIB\_READ\_ONLY) and instruction area ((SLIB\_INSTRUCTION), and it can be partially or completely used as the read-only area or instruction area.
- Data of the read-only area (SLIB\_READ\_ONLY) can be read by I-Code and D-Code buses but cannot be written.
- Program codes in the instruction area (SLIB\_INSTRUCTION) can only be fetched by MCU through I-Code bus (only executable), and cannot be read by reading access through D-Code bus (including ISP/ICP/debug mode or boot from internal RAM), for accessing SLIB\_INSTRUCTION by reading data operation will return all 0xFF or 0x00.
- Program codes and data in security library cannot be erased unless the correct code is keyed in. If a wrong code is keyed in, in an attempt of writing or deleting security library code, a warning message will be issued by EPPERR=1 in the FLASH\_STS register.
- Mass erase operation to the main Flash memory by end users will not erase the codes and data in security library.
- After sLib is enabled, users can also unlock the sLib protection by writing the previously defined password in the SLIB\_PWD\_CLR register. After the security library protection is disabled, the MCU will erase the whole main memory, including the sLib. Therefore, the program codes are protected against leakage even if the code defined by the software solution provider is leaked.

### 3.3 How to use sLib

For more details, please refer to " $AN0120\_AT32F425\_Security\_Library\_Application\_Note$ " from ARTERY official website  $\rightarrow$  Support  $\rightarrow$  AP Note  $\rightarrow$  AN0120.



## 4 Revision history

Date	Version	Revision note
2022.05.07	2.0.0	Initial release.
2022.07.11	2.0.1	Updated descriptions.
2022.10.11	2.0.2	Updated 3 <sup>rd</sup> party tools and added description of development environment and file paths.
2022.10.21	2.0.3	Updated description of UID and PID.

Table 1. Document revision history

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