

Guideline on AT32 MCU hardware design and ESD/EFT immunity design

Introduction

This application note is written to provide design guideline for hardware developers engaging in AT32-MCU based application solutions. On one hand, it gives an overview of compulsory hardware resources required for hardware design based on AT32 MCU, including power supply, clock and reset management, as well as debug ports. On the other hand, this document presents various design tips such as hardware and software design and PCB layout with the purpose of helping users enhance system's ESD and EFT immunity through design optimization. The last part aims to enable users to quickly identify possible causes in the face of typical failures.

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1 Power supply

For ensuring full-speed running and full-featured implementation, AT32 microcontroller requires an operating voltage supply (V_{DD}) which is defined in the appropriate data sheet. An internal LDO is used to supply the 1.2V digital power. The Real-time clock (RTC) and battery powered registers (BPR) can be powered by the V_{BAT} when the V_{DD} is powered off.

1.1 Independent ADC/DAC/CMP supply and reference voltage

To improve ADC/DAC conversion accuracy and comparator (CMP) robustness, an independent analog power supply pin (depending on the packages) is provided. With this pin, the ADC/DAC/CMP supply and reference voltage can be separately filtered and shielded from noise.

- ADC/DAC/CMP voltage supply is sourced from V_{DDA} pin
- A separate supply ground pin is provided on the V_{SSA}
- To allow for a better accuracy at low voltage inputs and outputs, the V_{REF+} (if available on packages) can be connected to a separate external reference voltage that is below the V_{DDA} . However, such reference voltage must be greater than the minimum V_{REF+} value.
- V_{REF+} can be connected to V_{DDA} . The V_{REF-} must be connected to V_{SSA} . They are internally connected to V_{DDA} and V_{SSA} respectively when the V_{REF+} and V_{REF-} are not available.

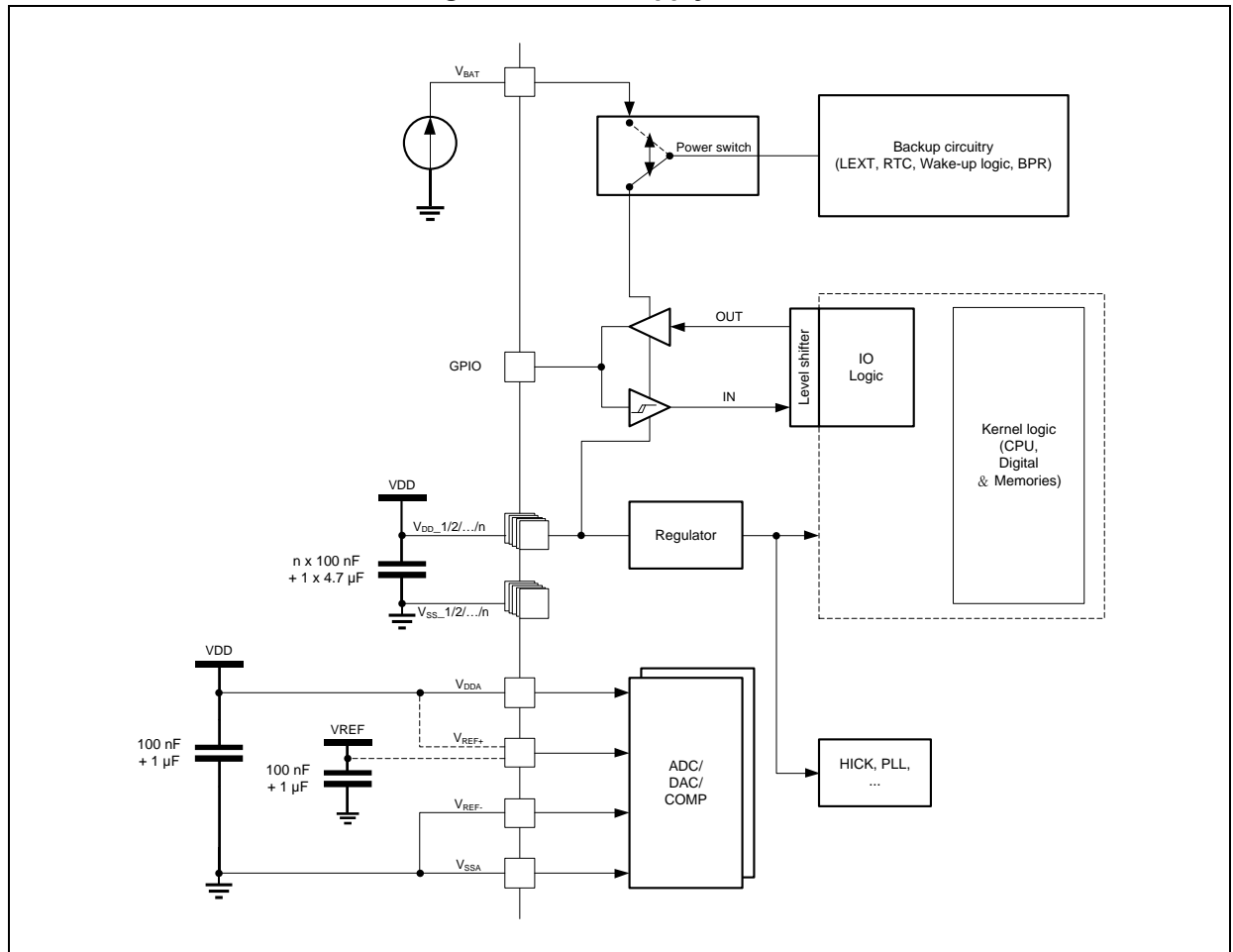
1.2 Battery power supply

To retain the content of the BPR registers and ensure RTC running when the V_{DD} is turned off, the V_{BAT} pin can be connected to a battery or another backup power supply. If no external battery is used in the application, then the V_{BAT} must be connected to V_{DD} externally.

1.3 Power supply scheme

- V_{DD} pin must be connected with an external decoupling capacitor (it can be a separate tantalum or ceramic capacitor of at least 4.7 μF . And each single V_{DD} must be connected with a 0.1 μF ceramic capacitor)
- V_{BAT} pin can be connected to an external battery. If no external battery is used, V_{BAT} pin must be connected to V_{DD} with a 0.1 μF ceramic capacitor
- V_{DDA} must be connected to two external decoupling capacitors (1 μF tantalum or ceramic capacitor + 0.1 μF ceramic capacitor)
- V_{REF+} pin can be connected to V_{DDA} . If V_{REF+} is to be linked to an external reference voltage separately, then it must be connected with two decoupling capacitors (1 μF tantalum or ceramic capacitor + 0.1 μF ceramic capacitor). The range of V_{REF+} must comply with the requirements defined in the “ADC/DAC characteristics” of the datasheet.
- More measures can be used to shield the analog power supply from noise, such as, by adding magnetic beads on the front of V_{DDA}/V_{REF+}

Figure 1. Power supply solution

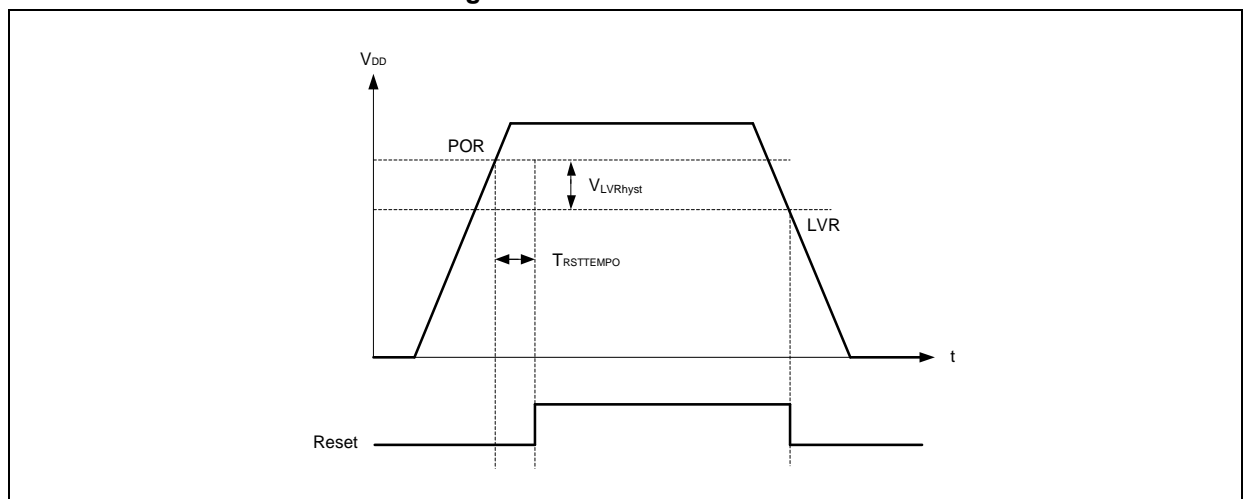


1.4 Reset and power supply monitoring

1.4.1 Power-on reset (POR)/low-voltage reset (LVR)

The AT32 MCU has an integrated POR and LVR circuitry which allows its proper operation when the V_{DD} voltage reaches V_{POR} . The device remains in Reset state when V_{DD} is below a specified threshold V_{LVR} , without the intervention of external reset circuit. For more details about the POR/LVR reset threshold, refer to the electrical characteristics of the datasheet.

Figure 2. POR/LVR waveform

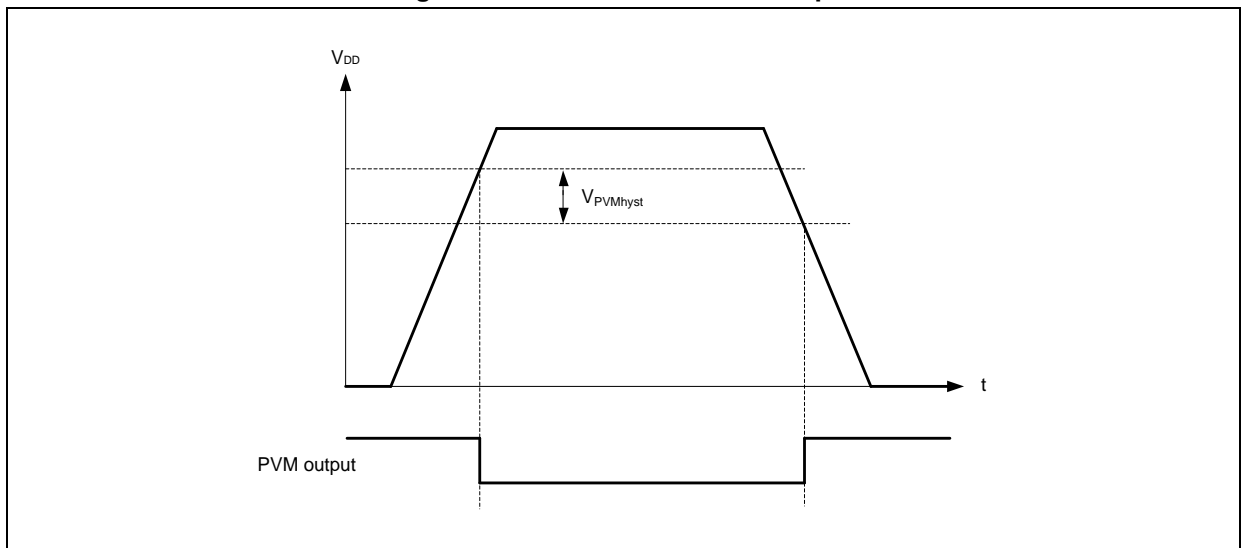


1.4.2 Power voltage monitoring (PVM)

The user can use the PVM to monitor the V_{DD} voltage by comparing it to the threshold selected by the PVMSEL bit in the power control register (PWC_CTRL).

The PVM is enabled by setting the PVMEN bit. The PVMOF bit in the power control/status register (PWC_CTRLSTS) is used to indicate whether V_{DD} is higher or lower than the selected PVM threshold. This event is internally connected to the external interrupt line 16 and can generate an interrupt if it is enabled through the external interrupt register. The PVM interrupt will be generated when V_{DD} drops below the PVM threshold and/or when V_{DD} rises above the PVM threshold, depending on the external interrupt line 16 rising/falling edge setting. A case in point is that this feature can be used to perform emergent shutdown tasks.

Figure 3. PVM thresholds and output



1.4.3 System reset

A system reset will set all registers to their reset values except the reset flags in the clock controller CRM_CTRLSTS register and battery-powered registers.

A system reset is generated when one of the following events occurs:

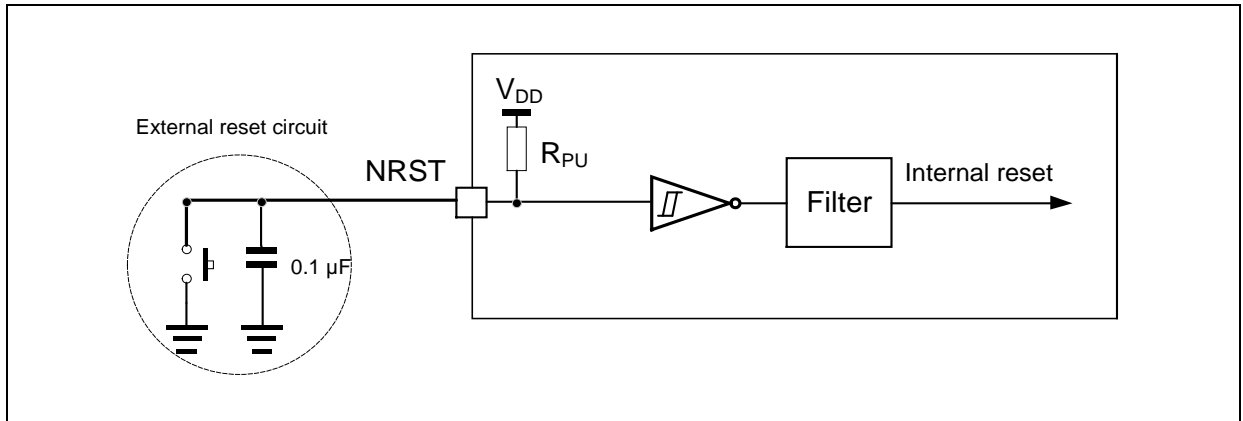
- V_{DD} drops below V_{LVR}
- A low level on NRST pin (external reset)
- Watchdog end of count (WDT reset)
- Window watchdog end of count (WWDT reset)
- Software reset
- Low-power management reset

The sources of reset events are indicated by reset flags in the CRM_CTRLSTS register.

1.4.4 NRST circuitry

It is highly recommend to connect the NRST pin to a 100 nF capacitor for better EMC performance. The NRST is internally pulled up to V_{DD} . A typical pull-up resistance is 40 k Ω , thus removing the need of an external pull-up resistor.

Figure 4. NRST circuit



2 Clocks

Three different clock sources can be used to drive the system clock (SCLK)

- HEXT high-speed external oscillator clock
- HICK high-speed internal oscillator clock
- PLL clock; PLL can be clocked by the HEXT or HICK

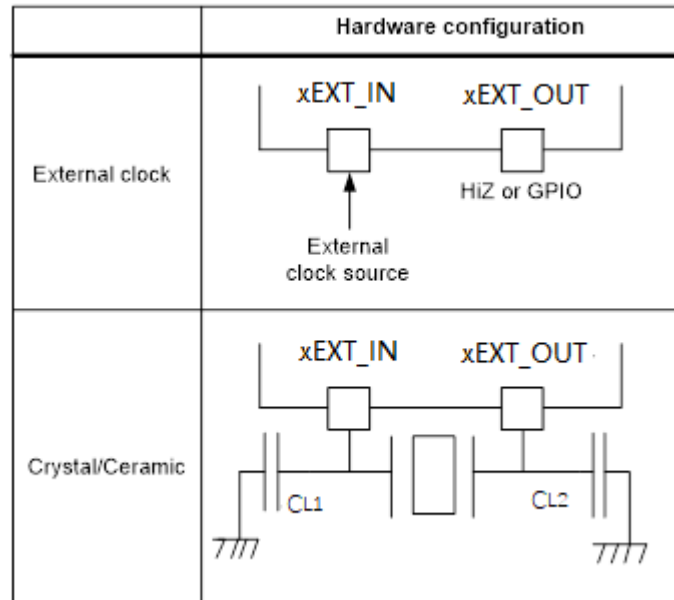
The devices have the following two secondary clock sources:

- Low-speed internal clock (LICK) which drives the watchdog and the RTC clock (RTCCLK) optionally used for waking up the system from DeepSleep/Standby mode
- Low-speed external crystal (LEXT) which optionally drives the RTC clock. Any clock source can be turned on or off independently when it is not used, in order to optimize system power consumption.

2.1 HEXT clock

The high-speed external clock signal (HEXT) can be generated from external clock source or crystal/ceramic resonator.

Figure 5. HEXT/LEXT clock sources



If external clock source mode is selected, an external clock must be provided and its frequency can be up to 25 MHz. The external clock signal (square, sinus or triangle with 45 ~ 55 % duty cycle) must be connected to the HEXT_IN pin while the HEXT_OUT pin should be left floating (some new products support the use of HEXT_OUT as GPIO simultaneously), see [Figure 5](#).

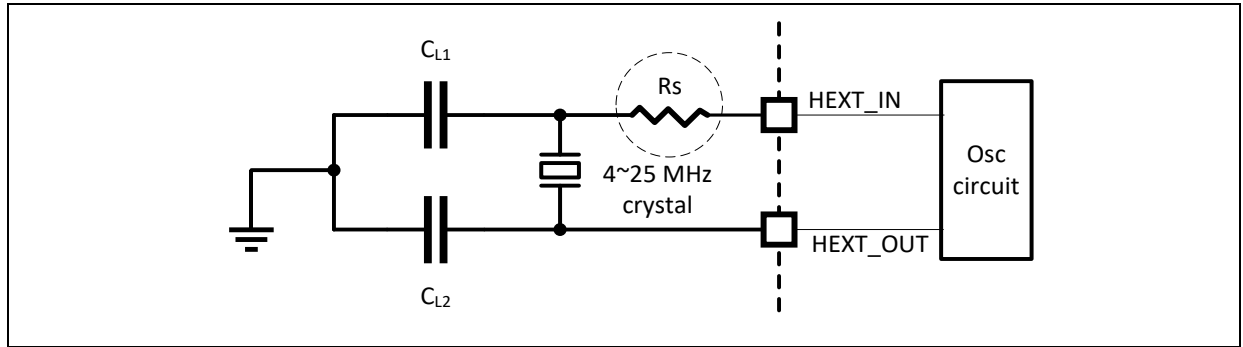
When crystal/ceramic resonator is used as a clock source:

- 4 ~ 25 MHz external crystal can provide more accurate main clock for the device. The crystal/ceramic resonator and the loading capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator. See [Figure 5](#).
- The crystal manufacturer typically specifies a loading capacitor C_L , which is the series combination of C_{L1} and C_{L2} . $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, in which the C_{stray} is a PCB and pin capacitance, in the 2 pF ~ 7 pF range.

For 8 MHz / 20 pF oscillator, its drive level (D_L) has a typical value of around 100 uW. If using a higher-frequency oscillator, its drive level will also be greater. When it comes to the reduction of the drive level, AT32L series is different from AT32F series in terms of operating methods. For AT32L series devices, you can select a lower drive level through related registers; For AT32F series devices, the only option is to connect them to external resistors in parallel or in series connection so as to reduce the drive level. The true drive level of an oscillator depends on the measurement of oscillator vendors.

Note: Given the design differences, for AT32F devices, the series resistor must be connected to HEXT_IN, instead of HEXT_OUT as usual. See Figure 6 below.

Figure 6. HEXT series resistor diagram



It should be noted that if MCU OTG master mode or CAN feature is used, for a better clock accuracy, the PLL which is generated by HEXT should be used to clock OTG master mode or CAN module. For USBFS or OTGFS device mode, they can be clocked by the HICK 48 MHz to save HEXT-related components and routes.

For more informations, refer to the electrical characteristics of the datasheet or reference manual.

2.2 LEXT clock

The low-speed external crystal signal (LEXT) can be generated external clock source or crystal/ceramic resonator.

The LEXT clock is a 32.768 kHz low-speed external crystal or ceramic resonator. It is capable of providing a low-power but highly accurate clock source to the real-time clock or other timing functions.

When crystal/ceramic resonator is used as clock source, the crystal/ceramic resonator and the loading capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator. See [Figure 5](#).

If external clock source mode is selected, its maximum frequency must not exceed 1 MHz. The external clock signal (square, sinus or triangle with 45 ~ 55 % duty cycle) must be connected to the LEXT_IN pin while the LEXT_OUT pin should be left floating (some new products support the use of LEXT_OUT as GPIO simultaneously), see [Figure 5](#).

For more informations, refer to the electrical characteristics of the datasheet or reference manual.

3 Boot mode

Three different boot modes can be selected through the BOOT [1:0] pin (depending on product model, it may be an external BOOT1 pin or the reverse value of nBOOT1 in the user system data) as shown in Table 1:

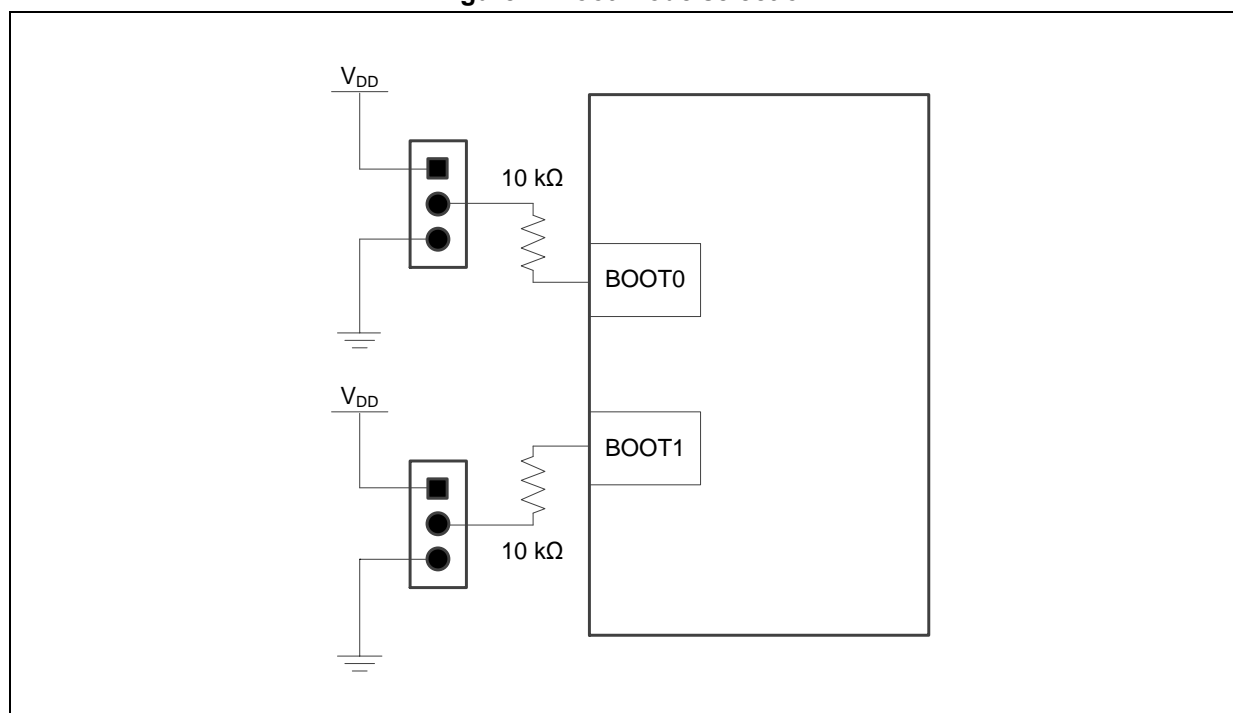
Table 1. Boot modes

Boot mode	Description	Configuration	
		BOOT1	BOOT0
Main Flash memory	Main Flash memory is selected as the boot space	X	0
Boot memory	Boot memory is selected as the boot space	0	1
SRAM	Embedded SRAM is selected as the boot space	1	1

The values on the BOOT pins are latched after a system reset. The user can select the required boot mode by setting the BOOT0 and BOOT1 pins after a reset. The BOOT values are re-latched when the device leaves the Standby mode. Therefore, the BOOT pins must remain in the required boot mode configuration when the device is in Standby mode.

Note: The BOOT0 has a fixed weak pull-down resistance of 75 kΩ which cannot be disabled.

Figure 7. Boot mode selection



4 Debug port

The AT32 MCU integrates the Serial Wire/JTAG debug port.

- Serial Wire Debug port (SWD)
- Standard JTAG Debug port (JTAG). Some products do not support the full functionality of JTAG, but SWO feature is still available.

Table 2. Debug port pin assignment

Debug port pin name	JTAG debug port		SWD + SWO debug port		Pin assignment
	Type	Description	Type	Description	
JTMS/SWDIO	I	JTAG test mode selection input	I/O	Serial Wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock input	I	Serial Wire clock input	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/SWO	O	JTAG test data output	O	Asynchronous trace	PB3
JNTRST	I	JTAG test reset	-	-	PB4

Figure 8. JTAG standard port circuit

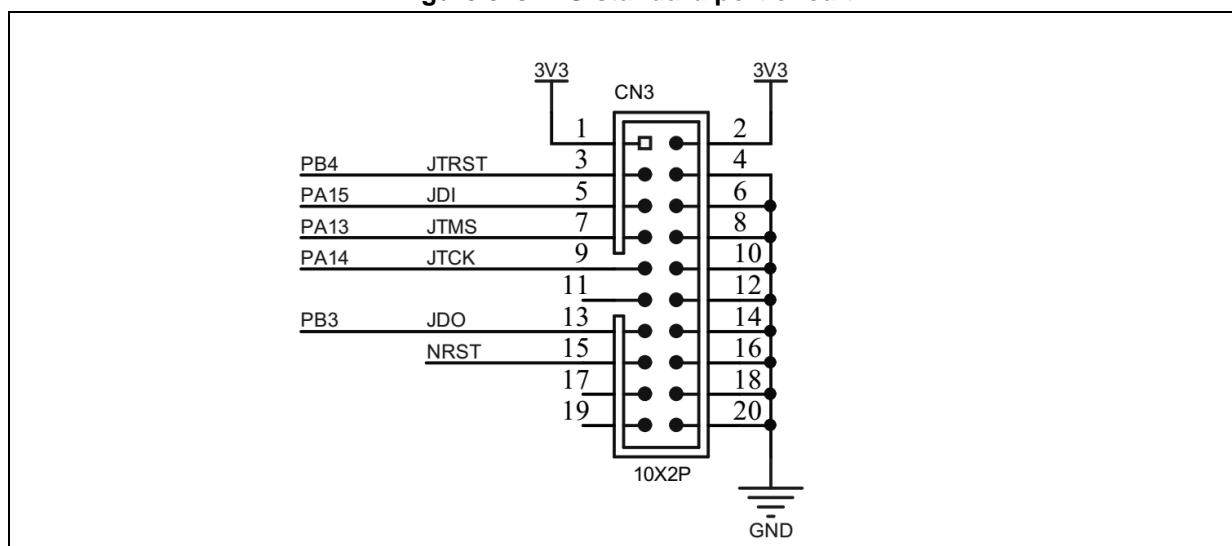
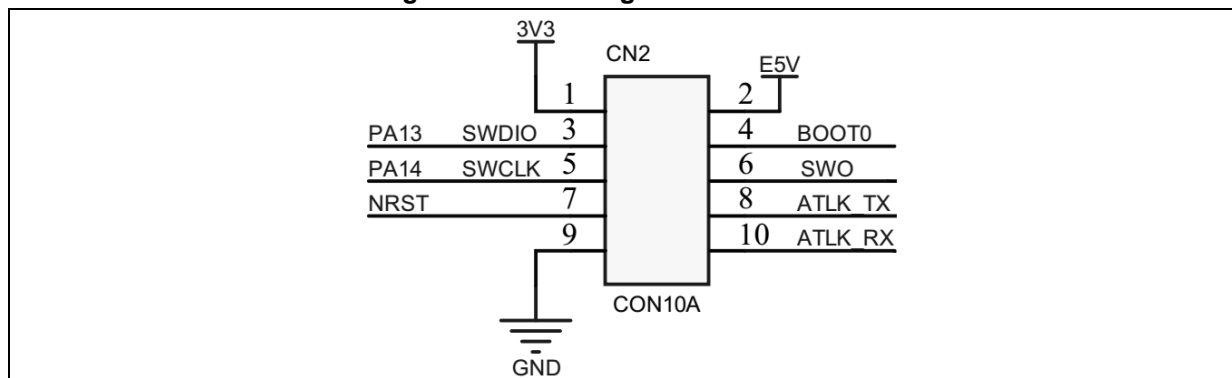


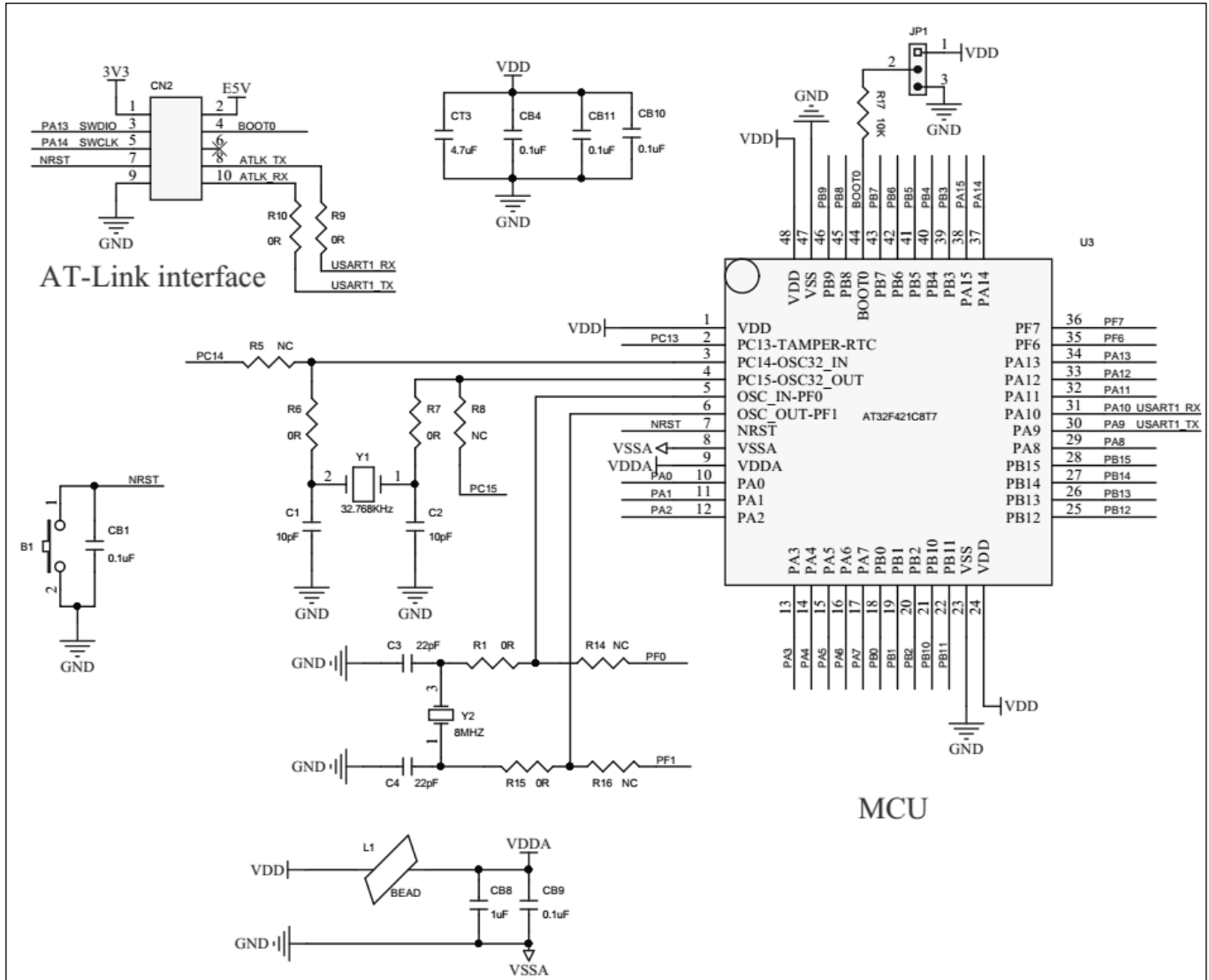
Figure 9. Combining SWD with AT-Link



5 Reference design

Figure 9 below takes AT32F421 series as an example. For more design information, refer to the AT-START evaluation board of the corresponding AT32 MCU series.

Figure 10. AT32F421C8T7 minimum system circuit



6 Schematic checklists

After the completion of the schematic design, the checklists below can be used for final check.

Table 3. Schematic checklist

Items	Description	Y, N, N/A
Power supply	Is V_{DD} pin voltage within spec?	<input type="checkbox"/>
	Are the voltages on V_{DDA}/V_{REF+} pins within spec?	<input type="checkbox"/>
	Are power pins connected with decoupling capacitors?	<input type="checkbox"/>
	Is the input voltage on V_{BAT} pin within spec?	<input type="checkbox"/>
	Is the V_{BAT} pin connected to V_{DD} if no external voltage source is used ?	<input type="checkbox"/>
Clocks	Is an external active clock signal input on HEXT_IN pin?	<input type="checkbox"/>
	Are the external active/passive clock frequencies within spec?	<input type="checkbox"/>
	Is the duty cycle of an external clock in the 45% to 55% range?	<input type="checkbox"/>
	Does the loading capacitance of a resonator comply with the manufacturer's spec? Are MCU pin capacitances taken into account?	<input type="checkbox"/>
	When OTG master mode or CAN feature is to be used, is there a HEXT crystal circuit as a system clock?	<input type="checkbox"/>
Reset	Is the NRST pin connected with 0.1 μ F ceramic capacitor?	<input type="checkbox"/>
Program and debug	Is the SWD/JTAG port connection correct?	<input type="checkbox"/>
GPIO pins	Are PC13/PC14/PC15 used as output pins with less than 3 mA drive current?	<input type="checkbox"/>
	Are all the sink/sourcing currents on GPIO pins less than 25 mA?	<input type="checkbox"/>
	Are the total amount of sink/sourcing currents on GPIOs less than 150 mA?	<input type="checkbox"/>
	Is the input signal level on GPIO pins within spec?	<input type="checkbox"/>
	Are FT pins not used when they are supposed to be? (such as 5 V CAN transceiver)	<input type="checkbox"/>
ADC	Is ADC input signal less than V_{REF+} ?	<input type="checkbox"/>
	Are the input impedances of ADC sample channels within spec?	<input type="checkbox"/>

7 Hardware design tips

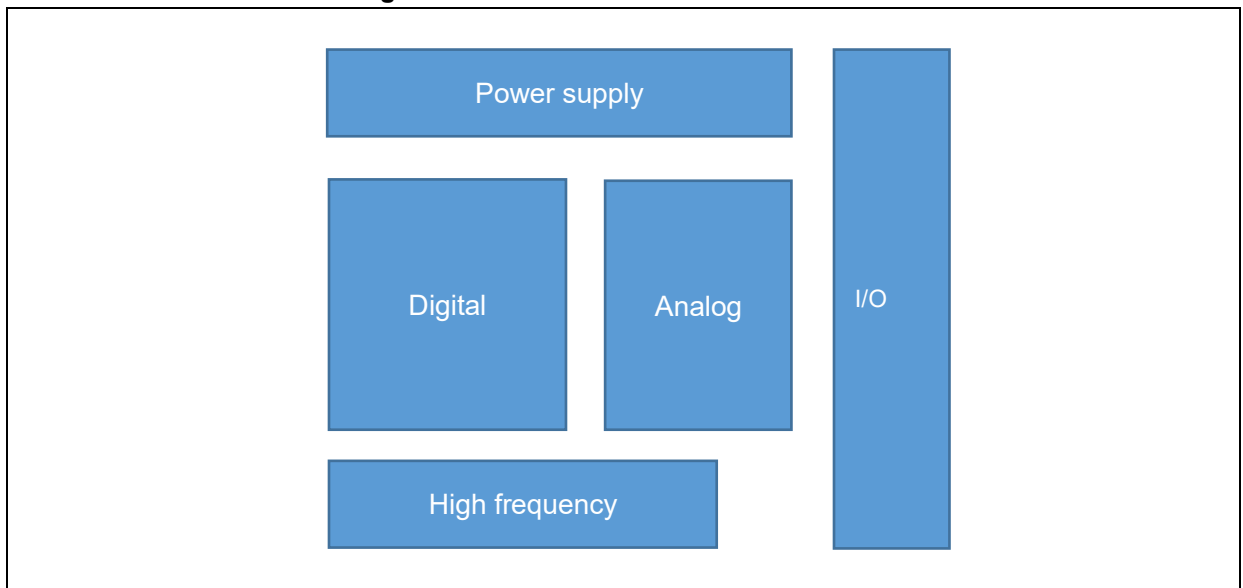
It is recommended that the users follow the rules described in the subsequent sections for circuit design and PCB layout in order to achieve better device performance and lower noise disturbance.

7.1 General PCB design tips

The layout design of PCB should take into account the placements of various functionality circuits and devices. For example, weak signal analog circuit, high-speed digital circuit and large noise circuit have to be separated from one another during PCB layout in order to minimize coupling interference from circuits. When it comes to the placements of devices, it is important to check if there is crossing or mixing issue among signal routes of different circuits.

- Voltage regulator and power supplies should be placed near power input port. Do not route the power signal line and high noise signal line in parallel
- Sensitive devices such as microcontroller and crystal should not be placed PCB edge; Instead, connection interfaces should be placed PCB edge
- Components within a functional module should be placed as close as possible to each other, so as to minimize their physical distances in between

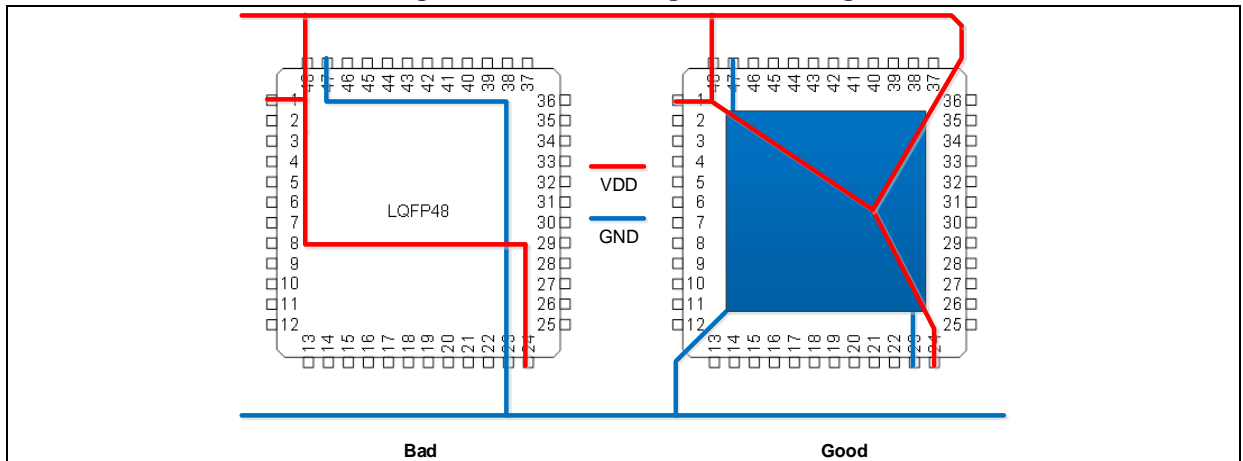
Figure 11. Placement of functional module



7.1.1 Power supply and ground

In most cases, the V_{DD}/V_{SS} pins should be routed in star-like mode (right below), not in chain-alike mode (left below). For multi-layer board, the V_{DD} pin is directly connected to internal power supply, while V_{SS} pin is directly connected to internal ground plane. It is recommended to place a digital ground plane just below the microcontroller.

Figure 12. Power and ground routing



Here are some recommendations for better EMC performance:

- Use multi-layer board
- Place one or two decoupling capacitors adjacent to power supply pins to reduce possible disturbance
- Use parallel capacitors set to expand the frequency range for filtering noise
- Ensure that only one star like node connects the analog ground with digital ground. This node should be placed as far as possible to MCU, but as close as possible to the bypass capacitor of a linear power supply regulator
- Isolate analog input signals through analog ground
- Minimize power and ground loop areas
- Ensure that at least two vias are available to connect power lines on different layers
- Apply protective components to the corresponding pins or port lines

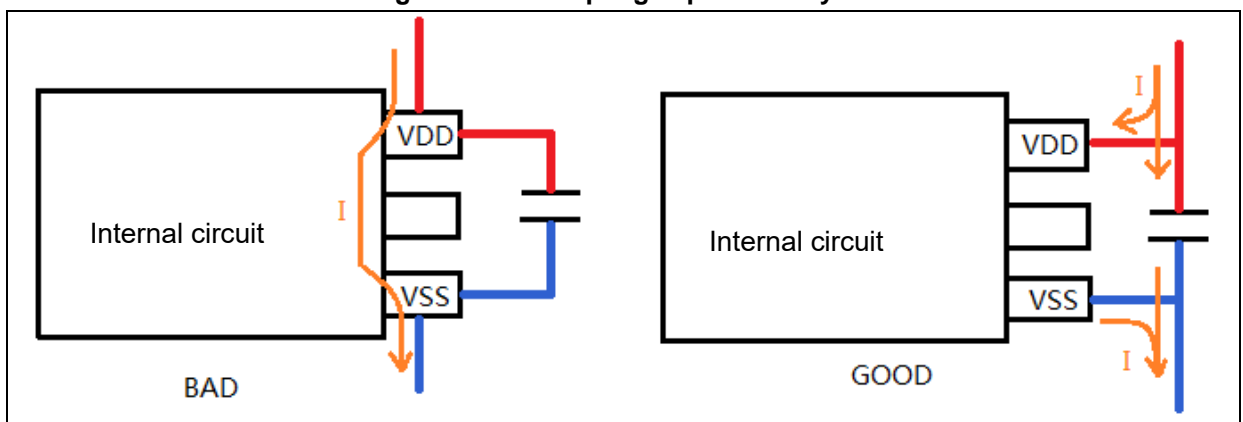
7.1.2 Decoupling capacitor

Decoupling capacitors must be as close to the V_{DD} pins as possible for the purpose of decoupling. A μF -level bypass capacitor should be placed at MCU's power input port (that is, along the line from PCB's LDO to MCU's power input port) to buffer voltage variations from public power lines and the noise from bypass power supplies. If a small ceramic capacitor and a large electrolytic capacitor are connected in parallel for decoupling purpose, the former (ceramic capacitor) should be placed as close to the V_{DD} pin as possible to minimize loop areas.

If possible, it is advised to place all decoupling capacitors on the same layer as MCU, or put them at the bottom layer under pairs of power pins (V_{DD}/V_{SS}).

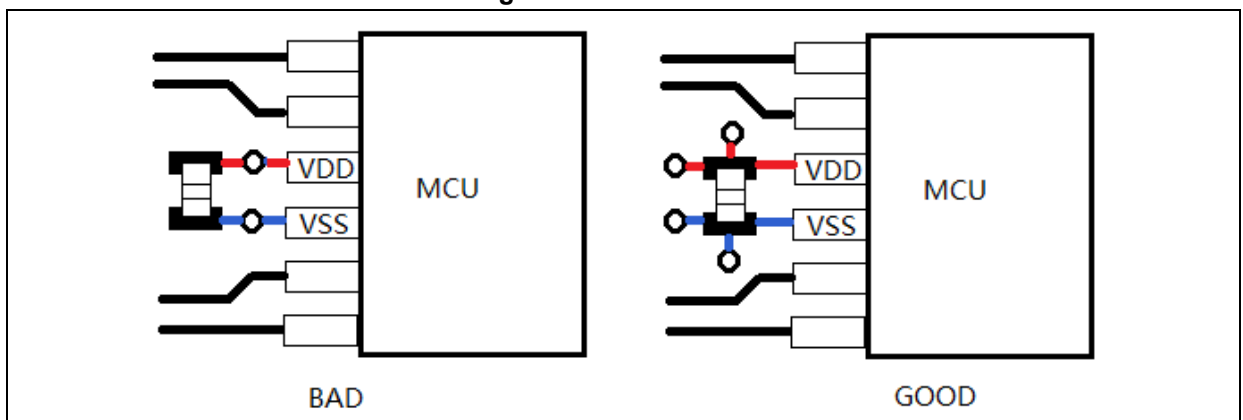
Power routing should first run through a decoupling capacitor pad and to V_{DD} pin so as to filter noise currents.

Figure 13. Decoupling capacitors layout



Power vias should not be placed between a decoupling capacitor and V_{DD} pin as this otherwise would invalidate the decoupling capacitor.

Figure 14. Vias location



7.1.3 Signal routing

After the completion of power and ground routing, priority should be given to crystal routing. Mixed or crossed routing should be avoided when there are mixed digital and analog signals in a circuitry. The layout of sensitive signals should be handled in the first place, and they should be protected against interference. For MCU peripheral circuits, the sensitive signals include clocks, reset and interrupt signal lines.

- Minimize the length of parallel routing
- If crossed routing is required for signals, they should be overlapped vertically to minimize decoupling capacitances arising from signals
- The distances among signal lines should comply with “3W” rule to minimize decoupling inductances

Additionally, USART/UART receive mode is relatively sensitive to the design of signal sampling. In most cases, they are normal in operation. But the start bit is likely to be deemed as invalid in severe disturbance environment so that data reception error may occur. As a result, it is recommended that a capacitor of 1~10 nF be grounded at RX pin, as close as possible to MCU side, with the aim of avoiding interference.

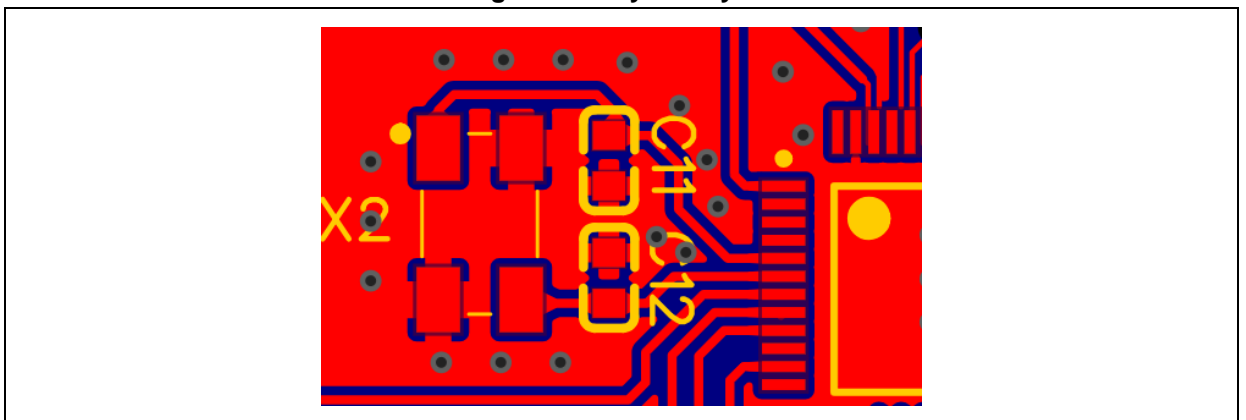
7.1.4 Crystals

The crystal oscillator is highly sensitive to disturbances at startup time. It is highly recommended that the crystal signal lines should not be placed in parallel with high current switching lines.

The general rules are as follows:

- A loading capacitor should be as close to the HEXT_IN/HEXT_OUT as possible and is protected with ground rings
- Signal lines (except ground line) should never be routed near crystal circuit or across the bottom-layer circuit
- Select a crystal with minimum frequency that meet system requirements
- Use a suitable loading capacitor
- Ground the crystal oscillator shell

Figure 15. Crystal layout



7.1.5 Analog signals

A weak analog signal is highly susceptible to digital signal. If both signals are required to be mixed, it is important to ensure that they are routed in an orthogonal way to minimize coupling effect.

If the V_{DDA}/V_{SSA} and V_{REF+}/V_{REF-} are not isolated from digital power and digital ground or not filtered, the ADC performance will be severely impacted.

7.1.6 Input/output ports

GPIOs in input mode are more sensitive to noise than in output mode.

To reduce external noise, it is advised to add a RC filter onto GPIO port that is configured as input mode. The filter should be placed as close to the GPIO pins as possible.

RC value depends on the characteristics of input signals. Typically, series resistance value is in the range of $100\ \Omega \sim 1\ \text{k}\Omega$, and filtering capacitance $1\ \text{nF} \sim 0.1\ \mu\text{F}$.

The layout where the NRST pin is externally connected to decoupling capacitors and pull-up resistors should be regarded as filter for power pins. As a result, the groundings loops of capacitors and V_{DD} loops of pull-up resistors should be minimized.

For unused GPIO pins:

- If GPIO pins remain floating, configure them as output low by software
- If GPIO pins are not floating, connect unused pins to a $10\ \text{k}\Omega$ pull-down resistor
- It is not recommended to connect unused GPIO pins directly to power supply or ground

7.2 QFN packages EPAD design tips

The QFN (that is Quad Flat No-lead) package is a surface mount chip scale package with small pad size and low profile. The QFN package, characterized by lightness, thinness, shortness and low profile, providing lower and competitive price. It also has the advantage of saving PCB area. In particular, its lead-less design allows itself to be free from concerns arising from pin damage caused during packaging, transportation and production, which often occur in lead package.

QFN main features:

- Surface mount package
- Light weight, suitable for portable applications
- Use smaller PCB area
- Good thermal performance with soldering pad at the bottom of the package

7.2.1 Thermal via design

There is a large area of exposed pad at the bottom center of QFN package. This pad is not only used to connect chip to ground, but also for dissipating thermal generated during chip running. For the same product, the θ_{JA} value with QFN package is usually lower than that of QFP or SOP package. In most cases, the EPAD is directly soldered onto a circuit board. The vias in EPAD help dissipate excessive thermal into copper ground layer.

For multi-layer PCB, the thermal can be transmitted to other copper layer through vias, thereby enhancing the capacity of chip to dissipate thermal.

7.2.2 Thermal via dimensions and placement

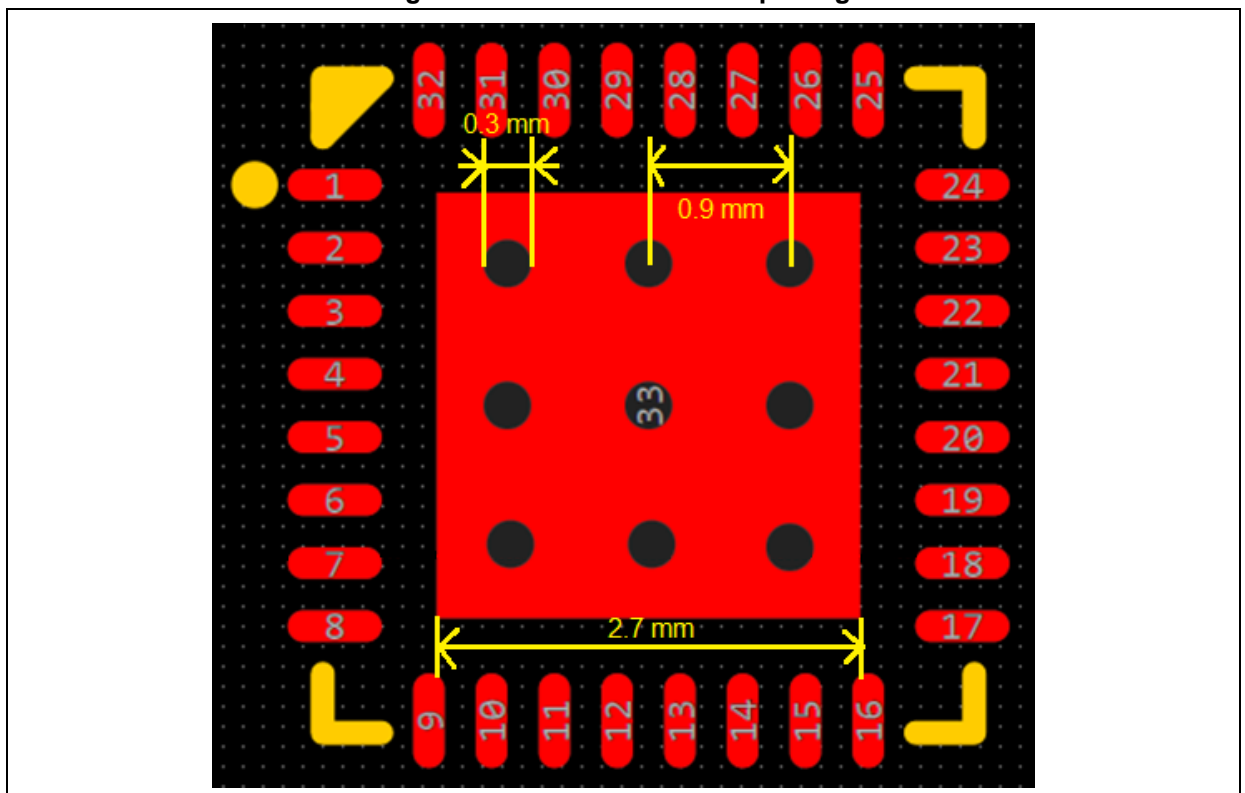
Theoretically, the greater the number of vias, or the bigger via diameter, the better the thermal conduction it generates. In other words, using more vias with bigger diameter often produce better thermal conduction. However, too large diameter is very likely to cause solder leakage and thus affect solder reliability.

Recommendations are as follows for via dimensions:

- Via Pitch: 0.8~1.2 mm
- Via Diameter: 0.3 mm

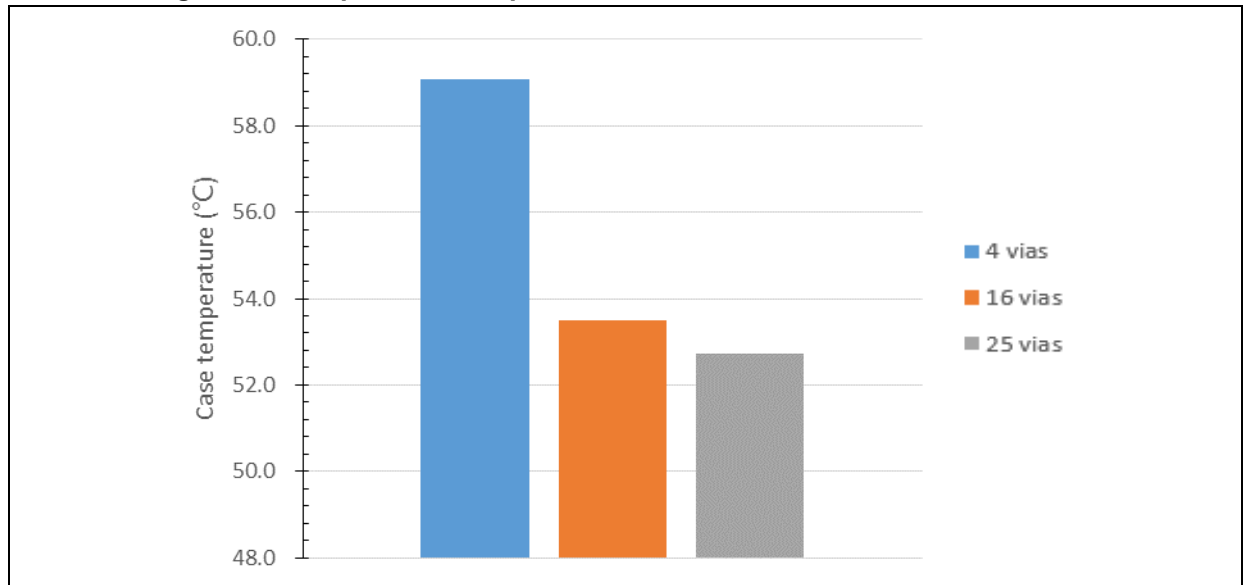
Based on this, taking QFN32 4 x 4 mm package as an example, Figure 15 shows the dimensions and placement of vias on QFN packages.

Figure 16. EPAD vias on QFN package



Taking AT32F435 QFN48 6 x 6 mm as an example, Figure 16 compares the temperature change when using different number of vias on EPAD. Under the same conditions, the internal chip temperature with 4 vias is higher than that with 16 and 25 vias.

Figure 17. Temperature comparison with different number of vias on EPAD



7.3 Other design tips

A robust system design should take into account both hardware layout and software design. Good system design, in conjunction with hardware configuration, can allow for a quick correction of system failures when they occur, and provide strong system protection by means of preventive features. Thus, it is important to guarantee system reliability by ensuring a close cooperation between software and hardware. This section gives some proposals for user reference. For more information, refer to the document [AN0041](#) or other related documents.

- Use watchdog to prevent system failure and code error
 - When a microcontroller is disturbed, program pointer jumps to an unexpected location or enters infinite loop. In this case, the watchdog will restart the system allowing it to return to normal. It is advised to refresh watchdog in main program rather than subprogram or interrupts.
- Define all interrupt vector functions, and add system reset sentences to the unused interrupt functions
 - If unused interrupts are triggered by false signals, software will jump to the defined interrupt function, and resume microcontroller after performing a system reset

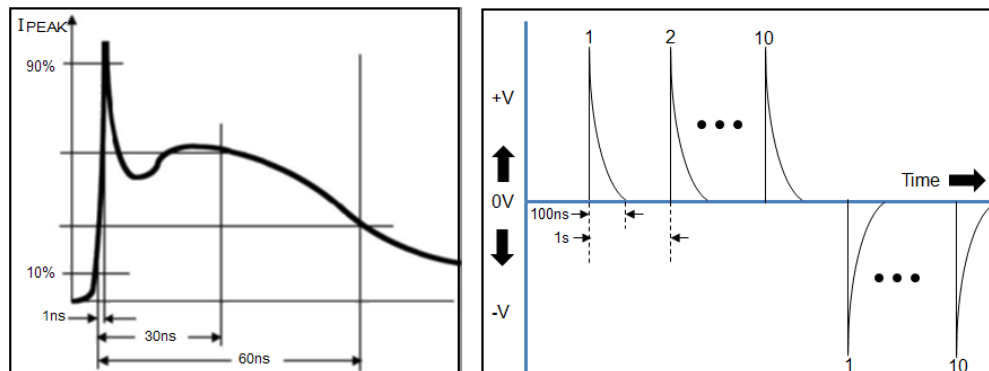
```
void HardFault_Handler(void)
{
    /* Go to infinite loop when Hard Fault exception occurs */
    while(1)
    {
        NVIC_SysReset();
    }
}
```

- Multiple-times access edge trigger event signals
 - Read the register value of the trigger signal several times in the interrupt function to judge whether it is a jamming trigger signal. It is possible to add a random delay between two read operations for the evenly distributed jamming signals.

8 ESD protection design tips

ESD is short for “Electro-static discharge”. It is a transfer of electric charge between bodies of different electrostatics potential in proximity or through direct contact. To put it simply, it means that a static charge moves from one surface to another. In the EMC field, it is called electrostatic discharge immunity test. More information can be found in the international standard IEC-61000-4-2/GBT-17626-2. ESD is divided into two categories: contact discharge and air discharge.

Figure 18. ESD contact discharge waveform



ESD effect

ESD cannot be completely eliminated but can be controlled. When an electrostatic charge occurs, there will be overvoltage, overcurrent and electromagnetic field to exist in the circuits. The overcurrent can cause direct harm to components. The electromagnetic field induced by ESD, is coupled to circuits and thus disturbs the normal operation of circuits, causing permanent or potential failures to components. All this unavoidable events will bring varying degrees of damages to MCU, thus having a negative impact on MCU performance. For this reason, it is important for our design engineers to take precautions or measures in advance to minimize or avoid such damages or losses from ESD.

8.1 ESD protection devices

8.1.1 Protection devices selection

Common protective components: TVS and ESD diodes

ESD diode shares the same operating principles as TVS diode, with their main differences being as follows:

- Different power and packages. The selection of TVS should take into account its power and package type. For ESD devices, select them depending on ESD rating (HBM/CDM) and level defined in IEC61000-4-2. Especially for high-speed signal traces, the capacitance of ESD diode must be included into consideration.
- ESD diode junction capacitance is smaller than TVS junction capacitance
- Different application scenarios. TVS is commonly used to perform primary and secondary protection, and ESD for board-level protection
- TVS can absorb large energy. It is mainly used to avoid surge on power input end, providing protection for back-end circuits by absorbing transient surge current;

ESD diode absorb less energy but enjoys fast response capability. It is capable of releasing static charge by connecting positive and negative ports to the power supply and ground, and connecting the common port to the protected pins.

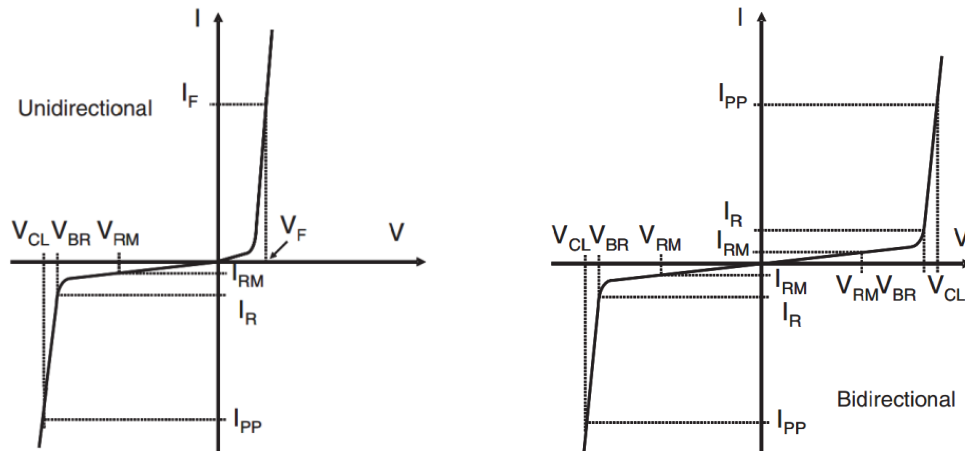
The following factors are taken into account when selecting protective devices:

- Depending on the polarity of protected signals, select whether to use a polarized unidirectional protective diode or bidirectional no polarity protective diode
- Depending on the maximum operating voltage of protected signals, select the clamping voltage value and maximum peak pulse current value of the protective diode
- Select the junction capacitance of the protective diode based on operating frequency and rising time of signals, as well as cut-off frequency for signal protection
- PCB design should be taken into account

8.1.2 Protection device parameters

Figure 18 shows the operating characteristics of unidirectional and bidirectional protection devices.

Figure 19. ESD/TVS operating characteristics



Reverse stand-off voltage, V_{RM} (also known as V_{RWM}): It refers to the maximum nominal operating voltage applied to a protection diode. At such voltage, the protection diode acts as a high impedance device, remaining in shutdown mode with an extremely low current leakage. This voltage must be greater than the expected peak working voltage of protected signals.

Breakdown Voltage (V_{BR}): At such voltage, the protection diode is turned on or already in connection state. V_{BR} is considered as the minimum value applied to a diode. It is usually higher than V_{RM} by 10 to 15 percent. This voltage is always higher than V_{RM} but lower than V_{CL} .

Clamping Voltage (V_{CL}): It is the clamping voltage that defines the voltage provided to a protected IC signal. Besides I_{pp} , the clamping voltage is one of the most important parameters that need to be taken into account when selecting a transient voltage suppressor.

Peak Pulse Current (I_{pp}): It refers to the maximum surge current a device is able to survive without damage. The peak pulse current represents a surge pulse of typically $8 \times 20 \mu s$ or $10 \times 1000 \mu s$.

Junction capacitance (C): The capacitor component is considered as a key parameter in the application scenarios requiring high-speed data processing. If a capacitance is too large, the quality and integrity of signals will be compromised. Thus high-speed signals such as Ethernet and high-speed USB require small-capacitance capacitors, usually less than 5 pF . In contrast, for medium/low-speed signals that need to be protected, a capacitor with larger capacitance is more useful.

8.2 Design tips

In actual applications, both TVS and ESD have their respective strengths so that users can make a suitable selection according to their needs. In addition, it is recommended that users should strengthen ESD protection through product structure design, for example, by using insulated materials to encapsulate circuit boards to avoid the shock from electrostatic charge.

8.2.1 Schematics

Filtering and protection for common GPIO lines:

Electrostatic transient interference is likely to be transferred to GPIO lines, directly or via power supply path. The following measures are recommended to protect against electrostatic transient shock.

- Add ESD diodes on to GPIO lines
- Add RC filter with a suitable cut-off frequency
- Encapsulated ground protection, physical shield

For the GPIO lines which inputs from external circuit board to a microcontroller (MCU), the RC filter should be placed as close to the MCU pins as possible, and ESD diode to the input ports of signals.

For the GPIO lines that output signals from MCU, the RC filter should be placed as far to the connecting port of circuit boards as possible. For unused GPIO pins, if floating, they should be configured as output mode with low level output; if not floating, they can be connected to ground via 10 k Ω resistor.

Filtering and protection for key signal lines

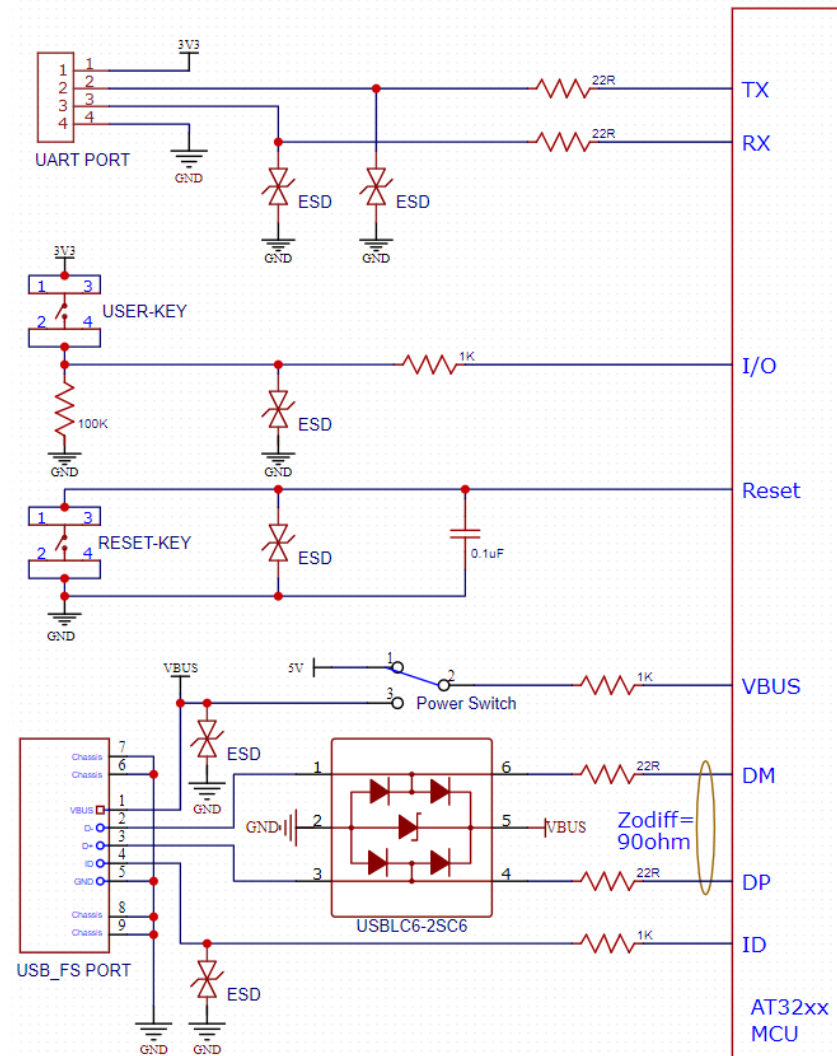
- For I²C and SPI communication lines, they can be in series connection with resistors. Such resistors, together with parasitic capacitance from routes and pins, serve as a low-pass filter to shield from high frequency noise. The series capacitors should be placed adjacent to pins, a typical value of 100 Ω ~ 330 Ω . Besides, a pull-up resistor can be installed, with its value depending on series resistors, clock speed and signal level.
- Even though the filtering capacitors on I²C and SPI lines can help shield high frequency noise, special attention should be paid to the fact that such capacitors are likely to affect the integrity of signals. Thus it is important to ensure that the rising and falling times of signals caused due to the addition of capacitors are within specifications.
- For UART communication line, it is possible to implement port protection through series resistors, ESD diode and isolation converter
- For reset and interrupt input lines, RC network can be used to protect against transient noise. Just as mentioned in the previous sections, it is possible to enhance system ESD/EFT protection by switching from edge trigger to level trigger, and judging trigger signals through many attempts in the interrupt functions. High frequency noise can be effectively filtered by adding pull-up resistors and pull-down capacitors to reset lines, and placing them close to NRST pins.

ESD protection circuit design example for common signal ports:

Figure 19 gives an example of ESD protection circuit for common signals, as a reference for users.

For ESD protection device, it is recommended that use selects ESD5311N-2/TR from Willsemi Company. The ESD5311N-2/TR is a 1-line, bi-directional, ultra-low capacitance transient voltage suppressor designed to protect high speed data interfaces from over-stress caused by ESD. For more information about this TVS, refer to its datasheet.

Figure 20. ESD protection circuit for common signal lines



8.2.2 PCB design

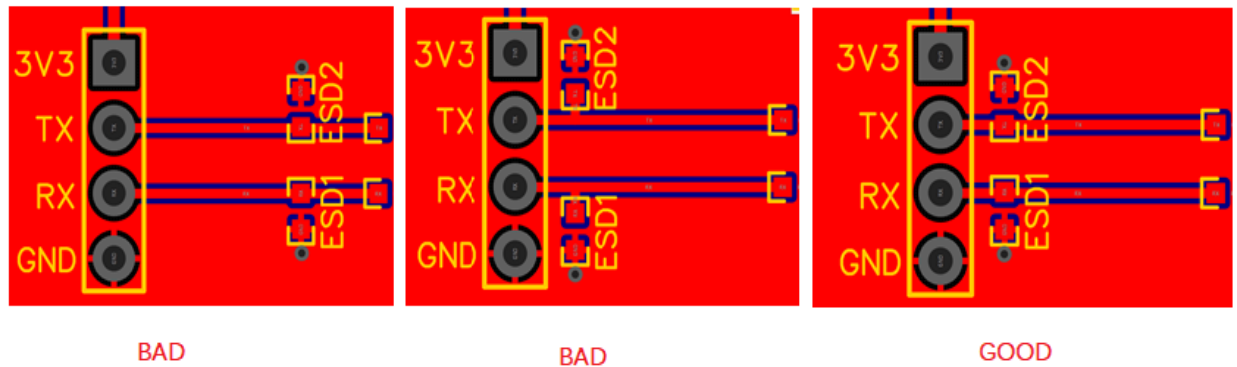
This section gives additional design tips on top of the descriptions stated in [Chapter 7](#)

PCB layout:

To get better ESD protection, the following points should take into account prior to PCB design:

- Minimize the loop area currents run through so that they are able to return to power source as soon as possible. In terms of PCB layout, it should be designed to have short-distance and low-resistance channels that facilitate the return of noise to the source destination. If the route resistance is larger, it may cause noise to be moved to the microcontroller and other circuits.
- The layout of circuits should take into account their respective functions, namely, analog, digital, power supply and GPIO. Sensitive devices such as controllers and crystals should be placed as far to PCB edge as possible.
- The V_{SSA}/V_{SS} and filtering bypass capacitors should be directly connected to ground plane (rather than through ground lines), and placed on the same side of the microcontroller.
- ESD devices should be directly (rather than through ground lines) connected to ground plane in order to minimize inductance. Besides, they should be placed as close to the external socket connectors and switches as possible.

Figure 21. ESD protection device layout comparison



Cautions:

- Never use a jumper or 0 Ω resistor to connect with ground plane as they will increase inductance of the return path of transient signals.
- Sensitive devices such as microcontrollers and crystals should never be placed near PCB edge
- If possible, use equidistant vias to connect with different ground layers to minimize inductances

8.2.3 Software settings

When it comes to ESD protection, in addition to hardware layout, software settings also play their important roles in this regard. To ensure the smooth operation of internal modules embedded in MCU can help strengthen ESD protection, in particularly in terms of system clock selection and PLL settings.

System clock selection:

When the applications allow, use HICK (internal clock) as the source of system clock or PLL. Compared to HEXT (external clock), the HICK is protected very well as its power supply or interfaces are not exposed, which allows it to receive less external disturbance and thus provides a relatively stable system clock.

PLL settings:

If HEXT is to be used as PLL input, high frequency noise is likely to be introduced via HEXT_IN/HEXT_OUT port and coupled to the VCO output of PLL and then to the system clock. In most cases, this high frequency interference goes beyond the operating frequency of MCU, thus causing unwanted results such as hardfault, program crash. Based on actual measurements, such interference can be effectively reduced by increasing PLL_FR value. The reason for this is that the PLL_FR (post-frequency division) can divide or average the VCO transient high-frequency output when the PLL is interfered so as to provide system with a stable clock.

As a result, increasing PLL_FR value can be used to protect against disturbance under the conditions that all PLL specifications are met. Additionally, if HICK is used as PLL input, it is still advised to configure a larger PLL_FR value even though HICK itself can provide better noise immunity.

8.3 ESD protection during chip use and storage

Microcontroller are sensitive devices to ESD. Therefore Artery has adopted a series of ESD protection measures during design and manufacturing. However, it is important for users to attach great importance to the protection of microcontrollers during their use and storage, in particularly in terms of electrostatic charge.

Electrostatic charge protection measures during chip use:

- Wear static-free clothing, shoes and wrists
- Install antistatic workbench, porcelain floor tiles, ceramic steel matrix laminated floors, etc.
- Use electrostatic eliminating device with ion generator

Their roles are to remove electrostatic charge imposed on human body.

Cautions: Never allow personnel without being equipped with protective measures to touch chip pins by hand.

Electrostatic charge protection measures during chip storage:

- Devices should always been stored in their original boxes
- If larger boxes are used to carry devices or PCB within short distance, they must be conductive, such as carbonaceous materials.
- Avoid using high dialectical materials (like polystyrene) for the assembly, storage and transport of devices

Electrostatic charge protection for equipment and tools:

- Use ionization blower to offset static charge from non-conductive materials
- Use soldering iron with good grounding function
- Use proper power supply during testing and use
- Insert and unplug sockets only when power supply is turned off

Additionally, ESD warning labels should be present and visible across the whole workspace, with regular check.

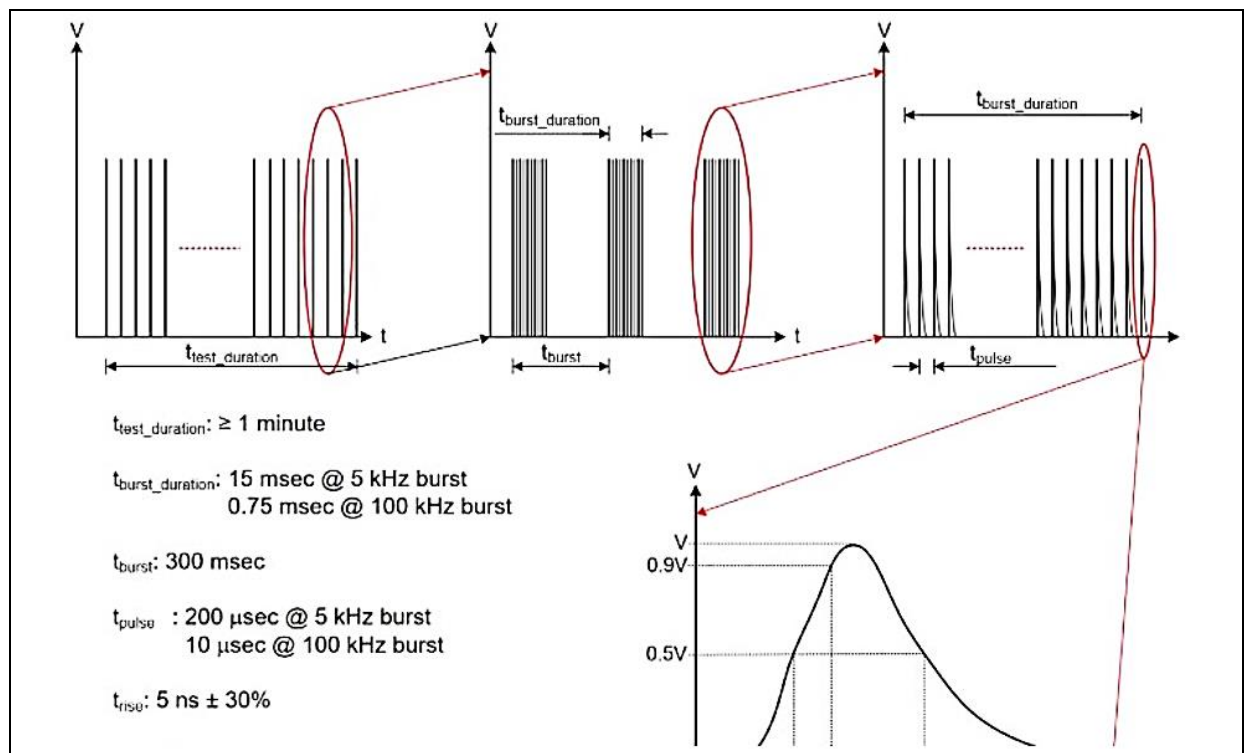
9 EFT immunity design tips

The EFT is short for “Electrical Fast Transient”. A standard EFT test is to monitor the operating status of the tested device by coupling disturbance pulses from external environment to the internal device. This test is designed to verify the devices’ capability to withstand fast transient burst under complex electromagnetic environment, and simulate the disconnection of adjacent inductive switches. For instance, sometimes we could see sparks when turning on an inductive switch. In this case, it can generate a pulse voltage of 2 ~ 4 kV, thus causing disturbances to surrounding products.

This pulse burst test is done by applying (coupling) many fast transient pulses to power, control and signal lines.

The electrical fast transient burst consists of successive pulse groups with 300 ms interval. Each pulse group lasts 15 ms. It contains many non-polar pulse waveforms. The rising edge of a single pulse is 5 ns. Each pulse lasts 50ns, 5 kHz in repetitive frequency.

Figure 22. EFT disturbance waveform



9.1 Failure type

The noise signals from electrical fast transient are coupled onto terminal devices via AC power lines, DC power lines and signal lines. If no proper actions are taken, such disturbances would be transmitted to microcontrollers and cause system failure.

The following items suffer most from electrical fast transient:

- Power supply and ground
- Reset circuit
- Clock and crystal circuit
- Communication circuits such as I²C/SPI
- High frequency digital and analog signals

Failure type caused by EFT test

- Reset

There are many factors contributing to MCU reset:

- Fast transient noise on reset pins could trigger external reset
- Disturbed power supply triggers power-down or power-up, or low-power reset
- Program crash triggers watchdog reset

Power-up, power-down and brown-out reset may occur under one of the following conditions:

- Power supply disturbance causes the pull-down of voltage
- Transient noise changes ground interference voltage
- Transient noise triggers ESD clamping circuit on GPIOs, reducing power supply voltage to microcontrollers and thus causing low power voltage reset
- Code jumps to unknown address or enters HardFault
- Latch up
 - Transient noise sends CMOS circuit into latch state by triggering ground bounce or changing reference voltage, which will fail circuits
- Communications failure
 - Corrupt signal integrity or trigger communication hardware failure
- Corrupt analog and digital signals
 - Transient noise causes glitches on digital signals, which will be treated as valid data pulses. The transient noise generated on analog signals will cause data distortion. In extremely cases, fast transient events can even change the status of MCU input and output ports, causing erroneous control signals.

9.2 Failure causes

It is important for us to identify failure causes and locations as this can help us optimize design to bolster EFT immunity.

Troubleshooting:

- Reset-related issue: first check the power supply of microcontrollers, and get reset type by reading RCC status register
- For latch up issue, check if MCU power consumption goes beyond a normal range
- For signals and clock issues, check if there are fast transient noise on related GPIO pins

An isolated oscilloscope is recommended to use for investigating EFT issues. The reason of this is that the oscilloscope grounding is likely to shunt noise signals so that the analysis results are not so accurate.

9.3 Design tips

9.3.1 Schematics

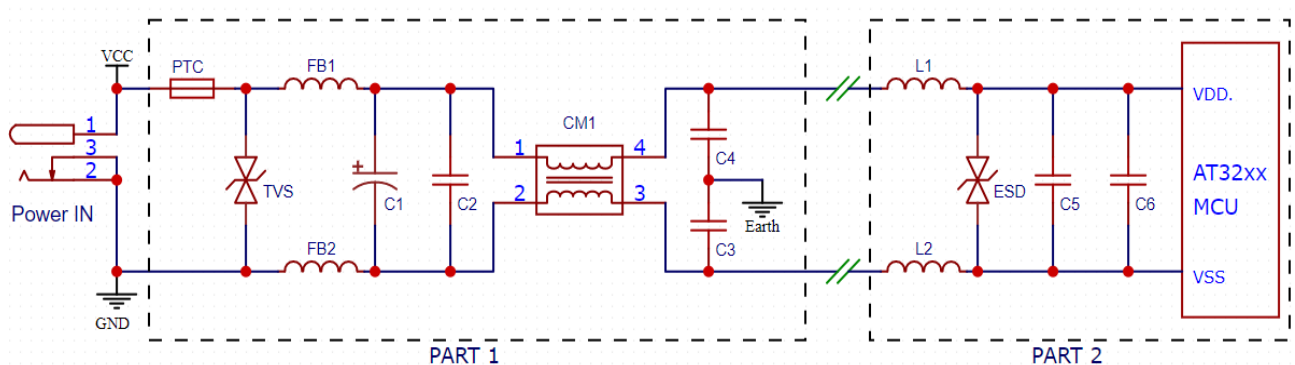
It is recommended to add TVS device on to power input port to strengthen anti-EFT performance.

TVS (transient voltage suppressor) has a larger capacitance than ESD diode, so its response time is slower than ESD. However, as TVS peak current is higher than ESD, it enjoys sound surge absorption, and that's why it is often added on power input port to absorb surge.

Example of power lines filtering and protection

Transient noise is usually introduced via power supply path. Thus it is important to apply a robust transient noise suppression mechanism to power lines. Figure 22 shows the location of filters on power supply route. In actual applications, users can select suitable filtering devices to meet EFT level of systems.

Figure 23. Recommended circuits for power supply filter and protection



In figure 22, “PART 1” should be placed as close to power input port as possible, while “PART 2” should be placed adjacent to MCU.

- PTC: POSISTOR
- FB1, FB2: Ferrite bead
- TVS diode. Refer to chapter 8 for more information about the selection of TVS.
- C1: bypass capacitor, typical value 0.1 μF ~ 1 μF
- C2: energy-storage capacitor, typical value 10 μF ~ 100 μF

- CM1: common mode choke, typical value 2 mH ~ 10 mH
- C3, C4: bypass capacitors connected to enclosure, typical value 0.1 nF ~ 1μF
- L1, L2: inductors, typical value 4.7 μH
- ESD: electrostatic charge protection diode, typical value ESD5311N-2/TR
- C5: filtering capacitor, typical value 1 μF
- C6: decoupling capacitor, typical value 0.01 μF ~ 0.1μF

9.3.2 PCB design

This section gives additional design tips on top of the descriptions stated in [Chapter 7](#).

PCB layout

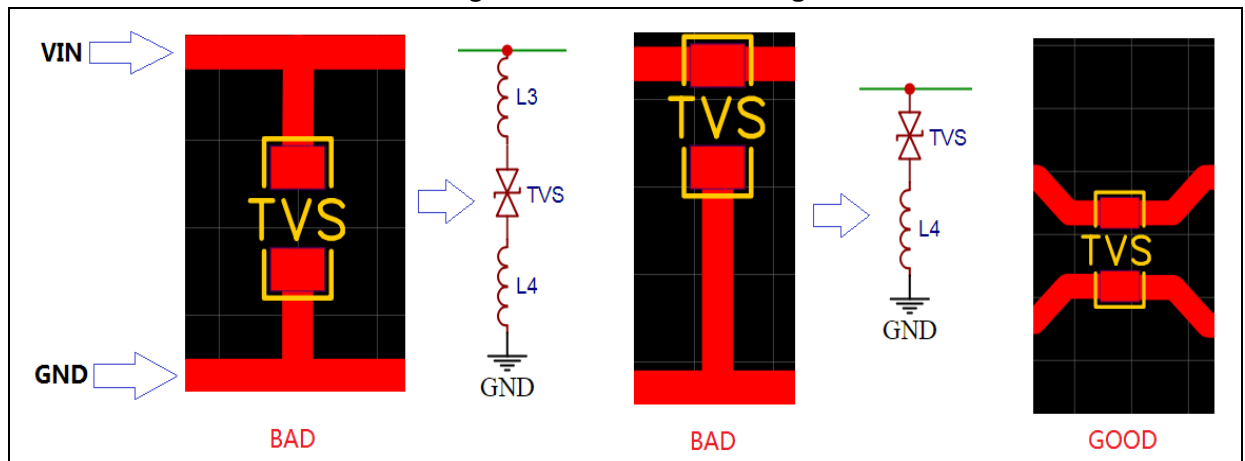
To get better ESD protection, the following points should take into account prior to PCB design:

- Minimize the loop area currents run through so that they are able to return to power source as soon as possible. In terms of PCB layout, it should be designed to have short-distance and low-resistance channels that facilitate the return of noise to the source destination. If the route resistance is larger, it may cause noise to be moved to the microcontroller and other circuits.
- The layout of circuits should take into account their respective functions, namely, analog, digital, power supply and GPIO. Sensitive devices such as controllers and crystals should be placed as far to PCB edge as possible.
- The V_{SSA}/V_{SS} and filtering bypass capacitors should be directly connected to ground plane
- TVS devices should be directly (rather than through ground lines) connected to ground plane in order to minimize inductance. Besides, they should be placed as close to the external socket connectors and switches as possible.

Line impedances

For high frequency signals, each line contains series impedance, series inductance and distributed capacitance from signal circuits. The routing should minimize the series impedances and series inductances of filtering and protection devices to provide better protection against EFT. For instance, line inductances are able to limit the valid bandwidth between decoupling capacitors and TVS diodes, and they can stop surge current when microcontrollers need a decoupling capacitor to replenish surge current.

Figure 24. TVS diode routing

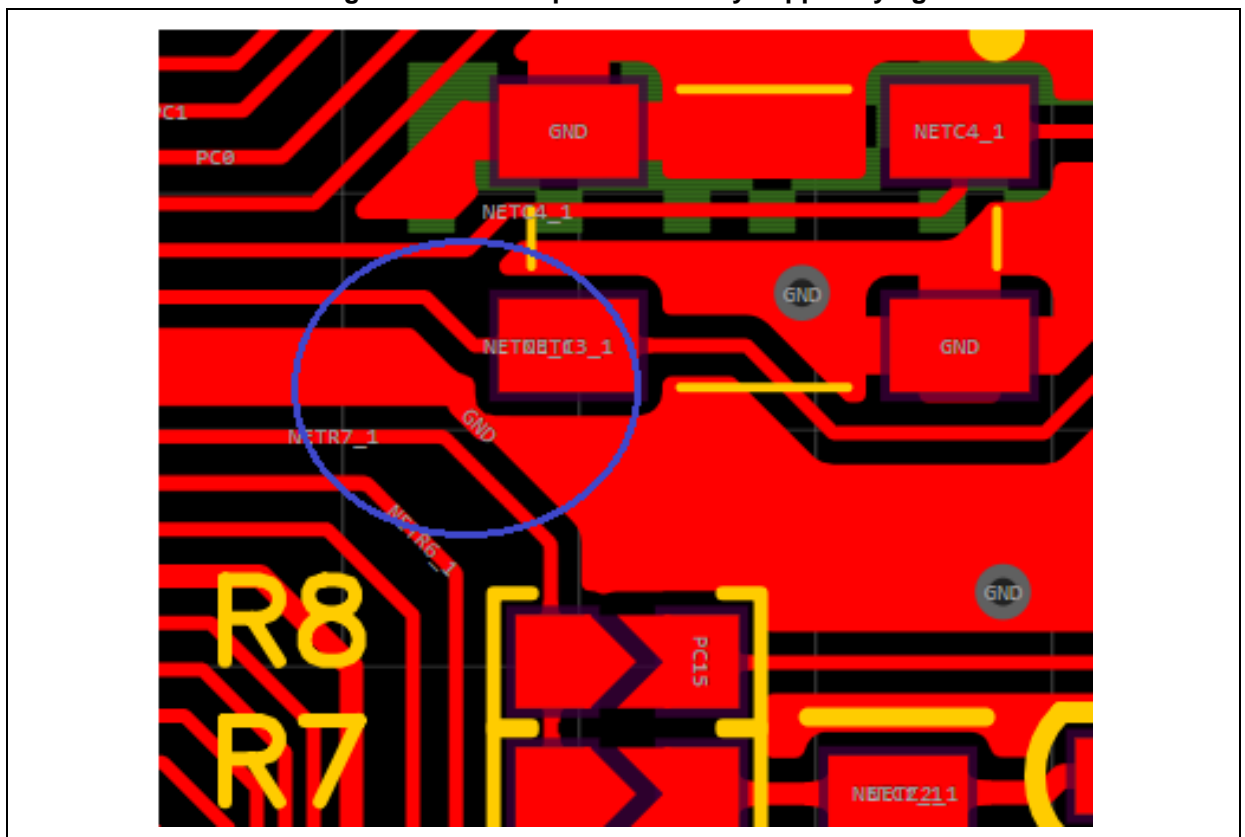


Grounding

Sound grounding is one of the most important parts in increasing anti-EFT protection. Ground loops are considered as major factors contributing to the transfer of transient disturbances as the impedances in transfer lines cause voltage difference between two devices. Ground plane is regarded as the most effective way to deal with transient disturbances. For the cost reason, it is also possible to use a local ground plane under sensitive devices. In whatever form, the final goal is to minimize the length between signal return path and power supply.

Special reminder: Do not just rely on laying copper to fill ground connection as this likely produces a narrow path with high impedance, which is very difficult to be detected without closer inspection. Therefore, it is recommended to first use routes to connect to ground path and then fill it with copper.

Figure 25. Narrow path caused by copper laying



Star-like grounding mode is useful for avoiding disturbance among different circuits through ground lines. If necessary, an isolation zone can be used to separate from sensitive circuits.

Three grounding modes

- Single-point grounding: parallel single-point grounding, rather than series single-point grounding, is recommended. The reason is that common mode resistances among reference ground planes of sub-module circuits may be coupled each other. Single-point grounding is more suitable for low frequency systems (less than 1 MHz) than high frequency systems as the latter has more ground loops which is likely to cause EMI problems.
- Multipoint grounding: this mode is suitable for high frequency systems as it can minimize loop currents and plane impedances and deliver sound EMI performance.
- Hybrid grounding: select appropriate grounding modes depending on functional modules. For instance, single-point grounding for analog circuit, and multipoint grounding for digital circuit.

Cautions:

- Never use a jumper or 0 Ω resistor to connect with ground plane as they will increase inductance of the return path of transient signals.
- Sensitive devices such as microcontrollers and crystals should never be placed PCB edge
- If possible, use equidistant vias to connect with different ground layers to minimize inductances

9.3.3 Software settings

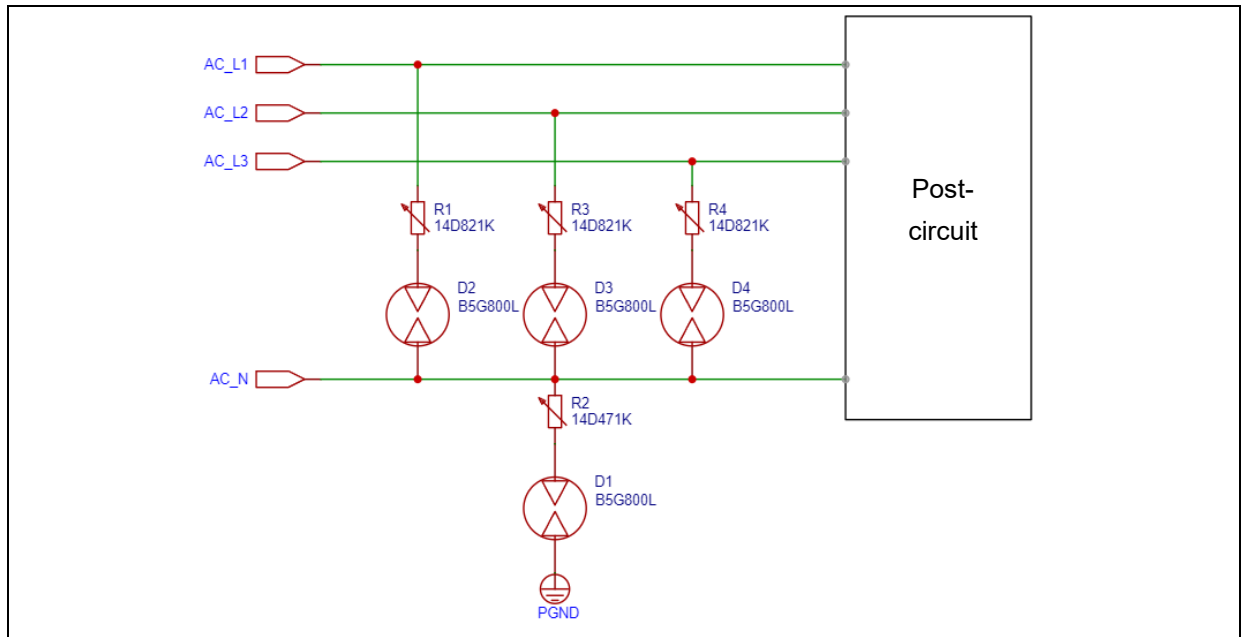
Like ESD disturbances, EFT is also able to bring external interference to internal chips. The software settings related to EFT are the same as those of ESD. Refer to [Section 8.2.3](#) for more information.

10 EMC typical hardware design

This section describes the typical hardware design for protection of ESD, EMI and EFT. The selection of the hardware circuits depends on the actual application scenarios and test requirements in order to achieve a tradeoff between design cost and performance.

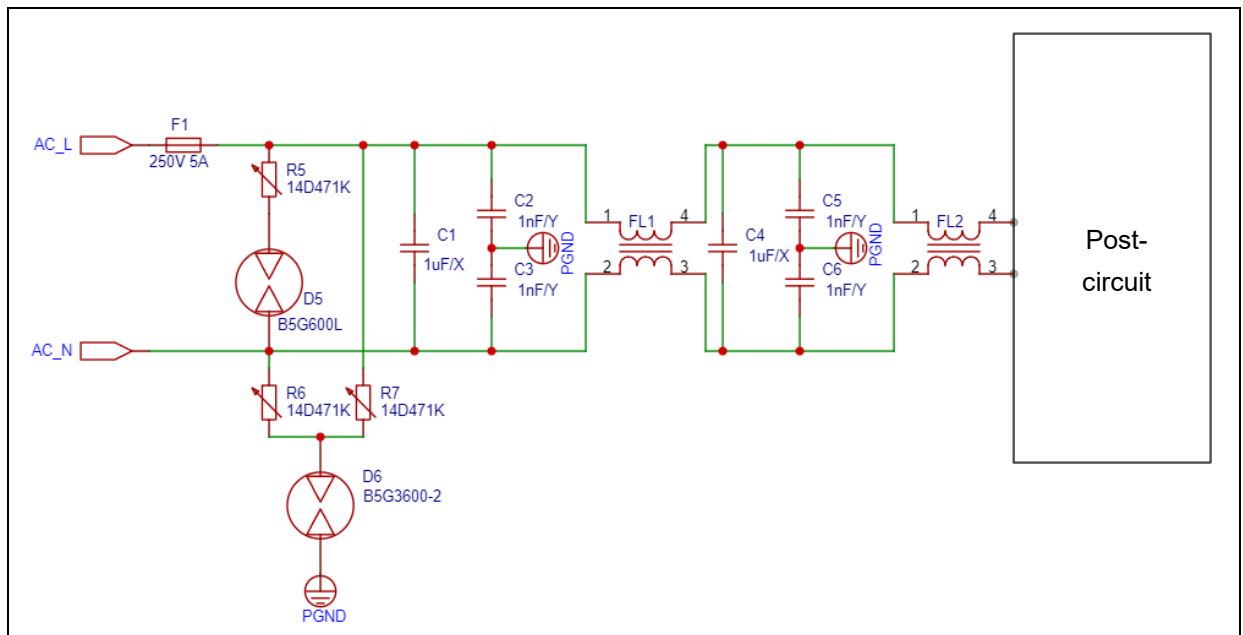
10.1 EMC design example for AC power supply

Figure 26. 380 V AC power supply



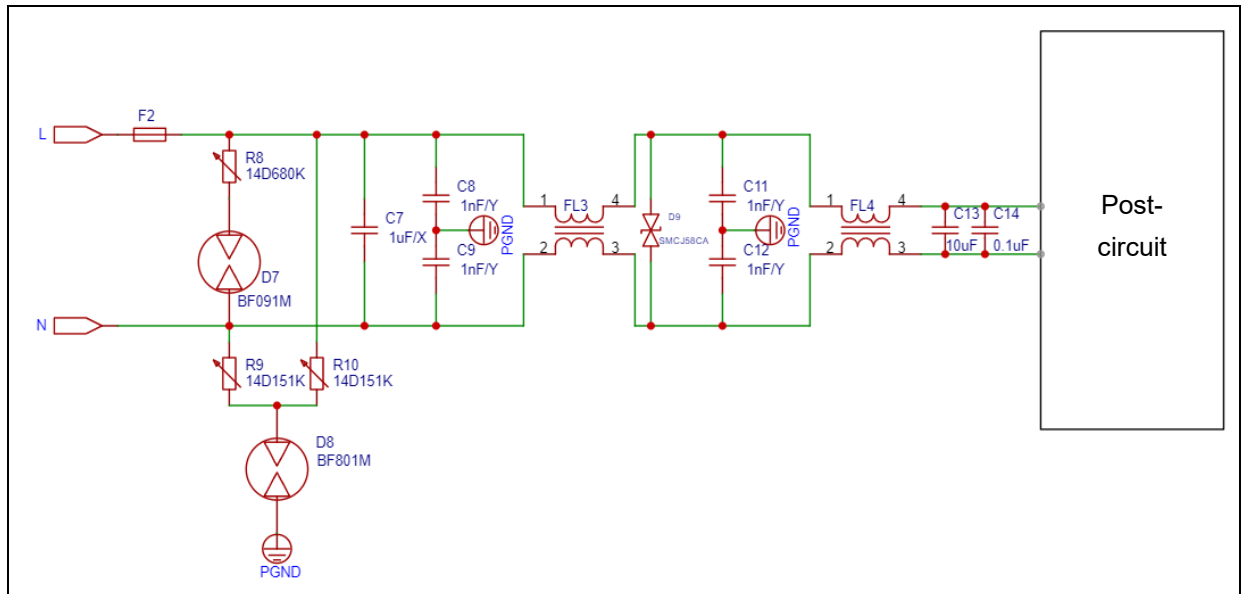
- This circuit meets 8/20 μ s test waveforms, 5 kA current capability, ± 5 times test

Figure 27. 110/220 V AC power supply



- Common mode inductor is selected depending on the working current of the product
- FL2/C4 are selected depending on EFT test level
- F1 selection depends on current and voltage
- This circuit meets 8/20 μ s test waveforms, 6 kV differential-mode voltage, and 6 kV common-mode voltage

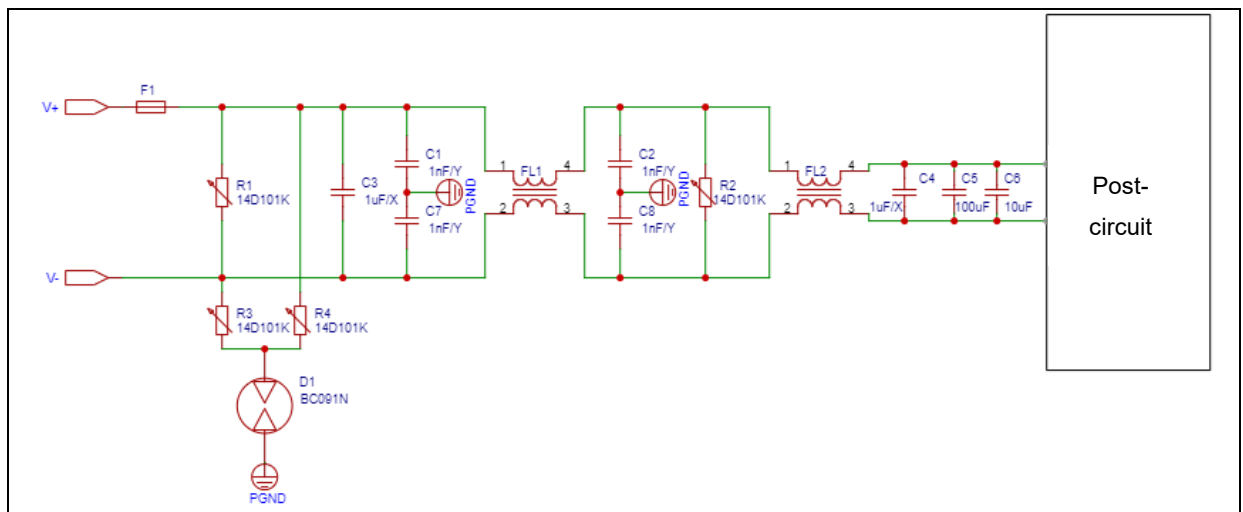
Figure 28. 24 V AC power supply



- Common-mode inductor is selected depending on the working current of the product
- This design offers surge protection, ESD protection, EFT, and conduction to choose according to test items
- D8 selection depends on the test voltage of the insulation resistance

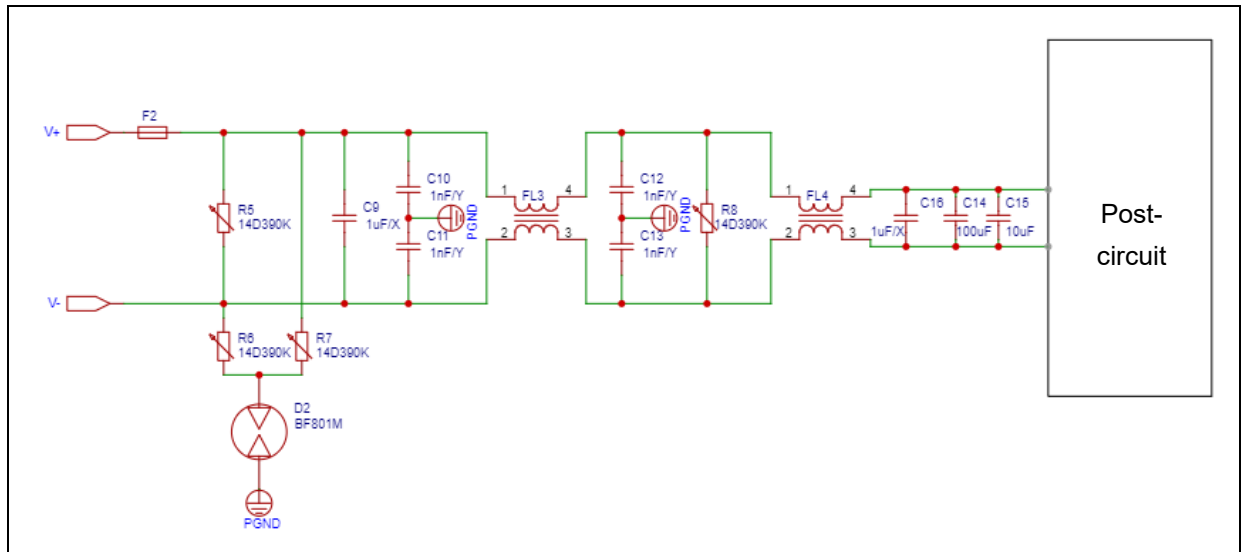
10.2 EMC design example for DC power supply

Figure 29. 48~72 V DC power supply



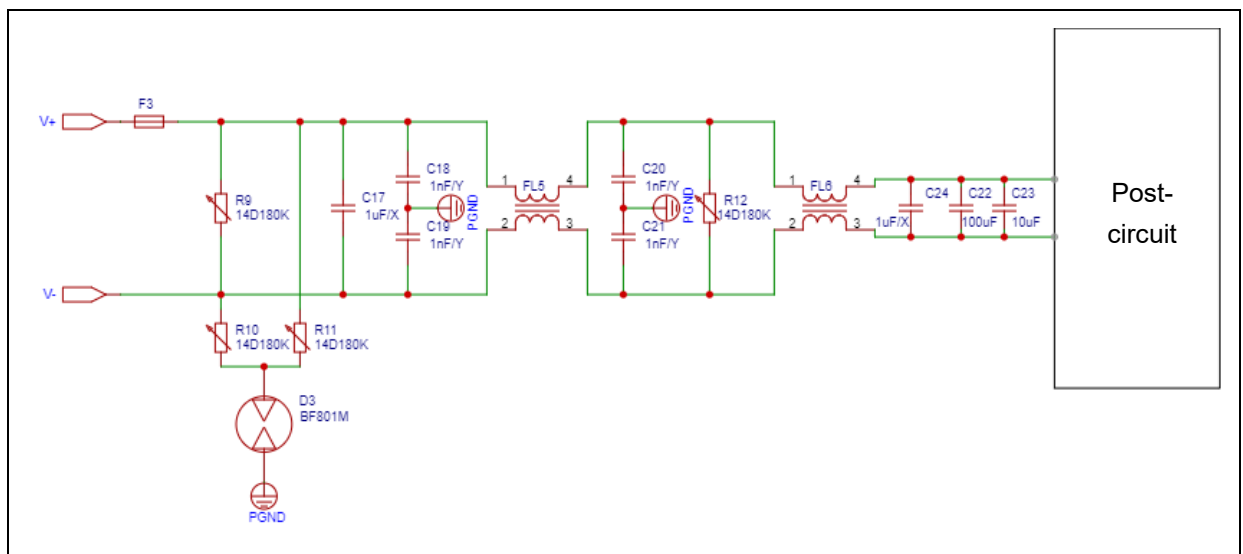
- Common-mode inductor is selected depending on the working current of the product
- This design offers surge protection, ESD protection, EFT, and conduction to choose according to test items
- D1 selection depends on the test voltage of the insulation resistance
- PGND represents the chassis earth

Figure 30. 24 V DC power supply



- Common-mode inductor is selected depending on the working current of the product
- This design offers surge protection, ESD protection, EFT, and conduction to choose according to test items
- D2 selection depends on the test voltage of the insulation resistance
- PGND represents the chassis earth

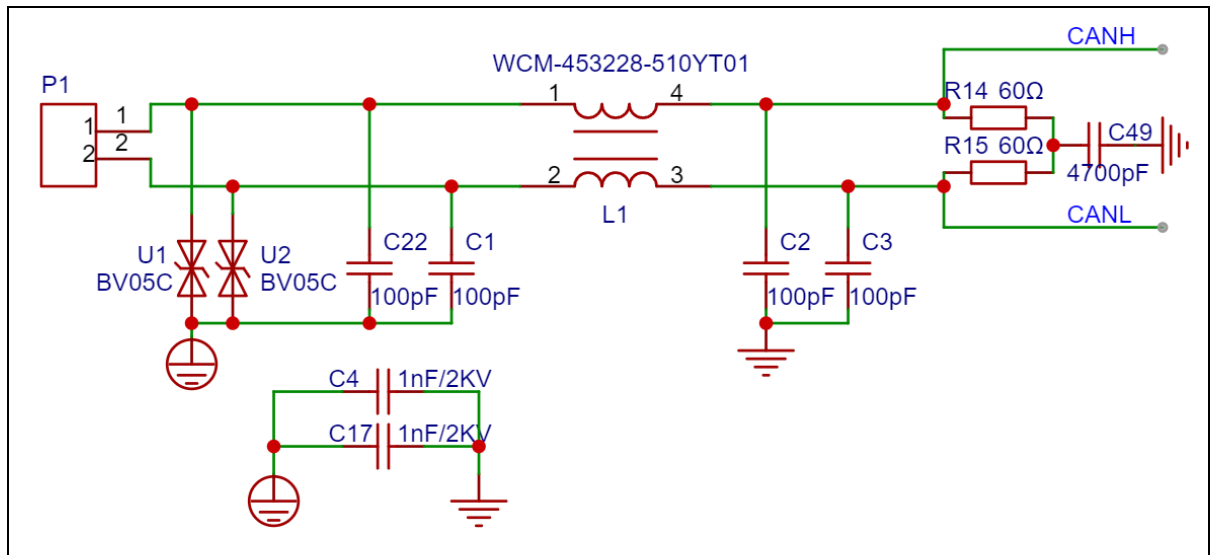
Figure 31. 12 V DC power supply



- Common-mode inductor is selected depending on the working current of the product
- This design offers surge protection, ESD protection, EFT, and conduction to choose according to test items
- D3 selection depends on the test voltage of the insulation resistance
- PGND represents the chassis earth

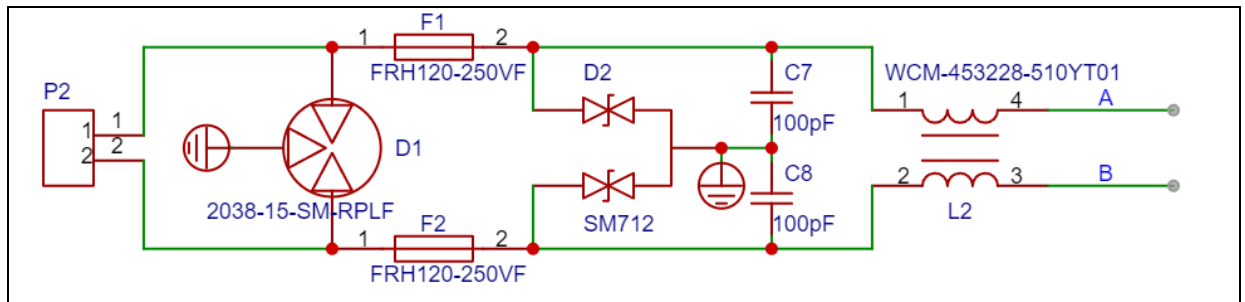
10.3 EMC design example for signal interfaces

Figure 32. CAN interface



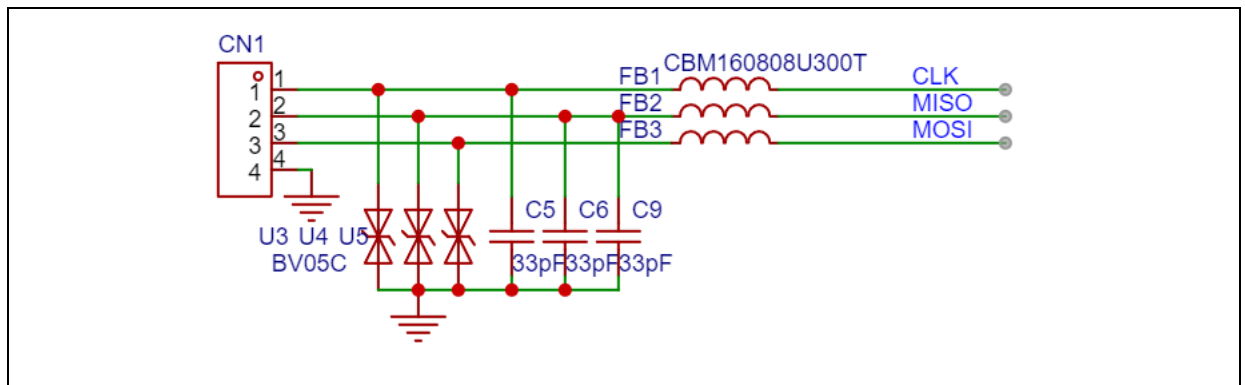
- TVS (U1/U2) and C1/C22 are connected to the chassis earth and placed close to the external connectors
- No ground pour below the common mode inductor L1

Figure 33. RS485 interface



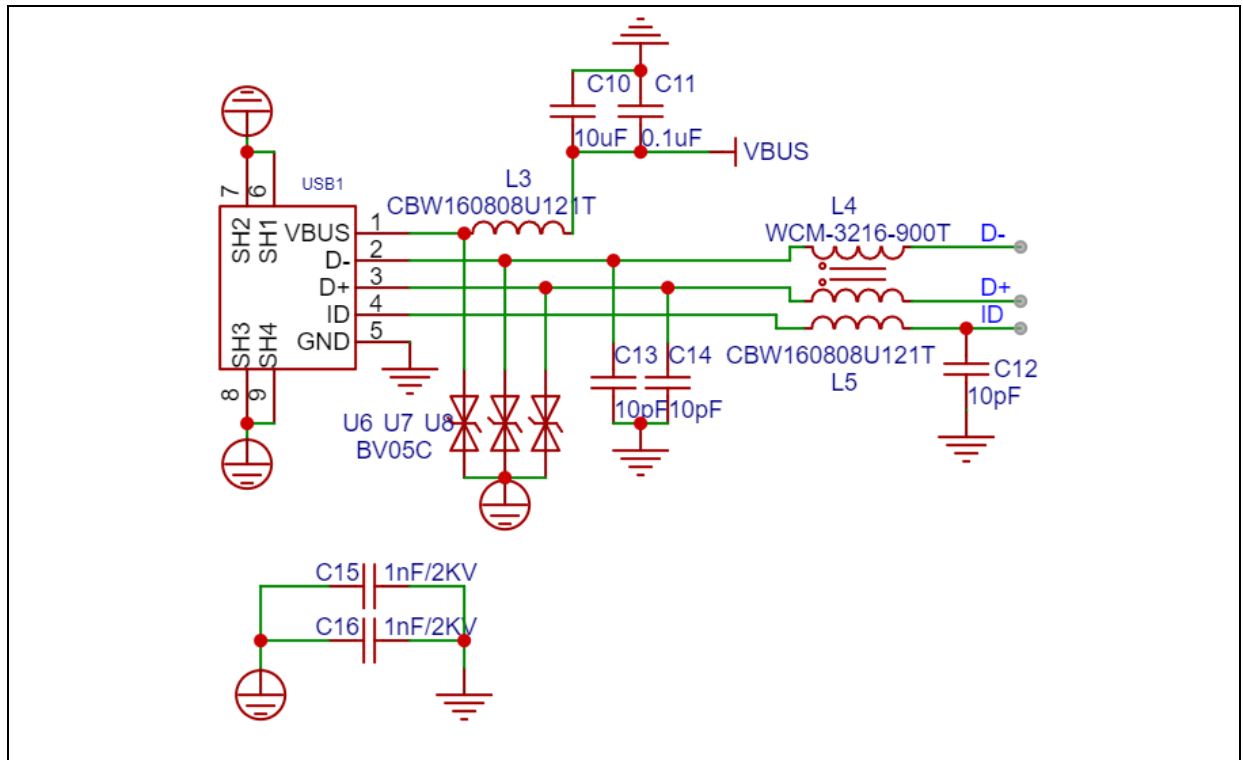
- D1/D2/C7/C8 are connected to the chassis earth and placed close to the external connectors
- No ground pour below the common mode inductor L2

Figure 34. SPI interface



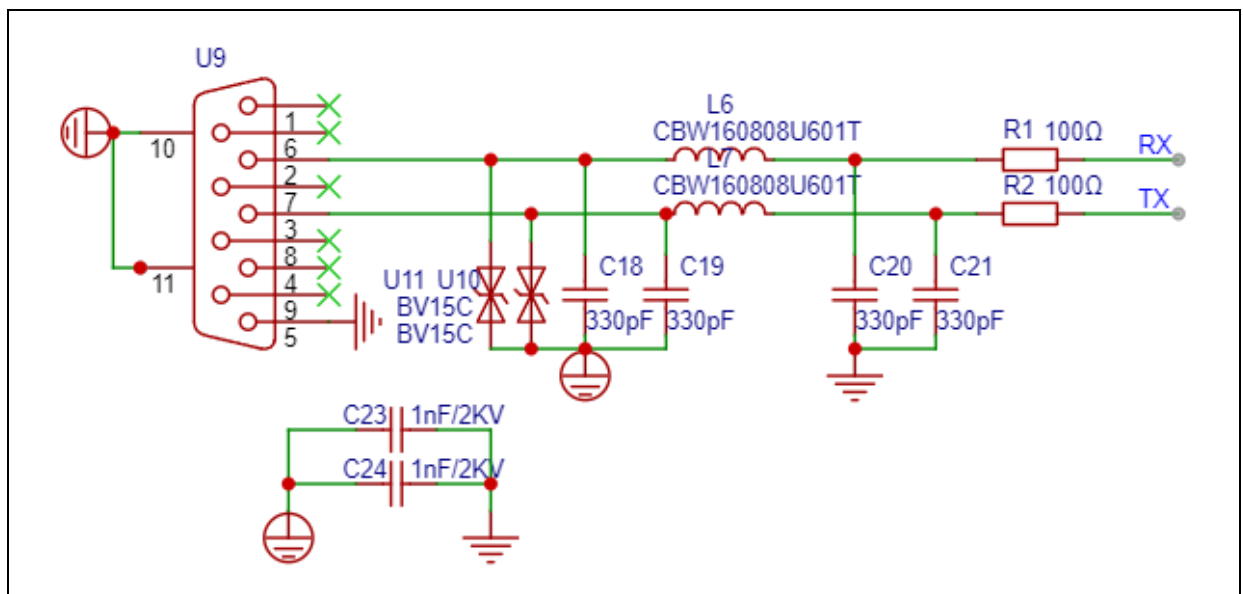
- FB1/FB2/FB3 and C5/C6/C9 are adjustable according to test results

Figure 35. USB2.0 interface



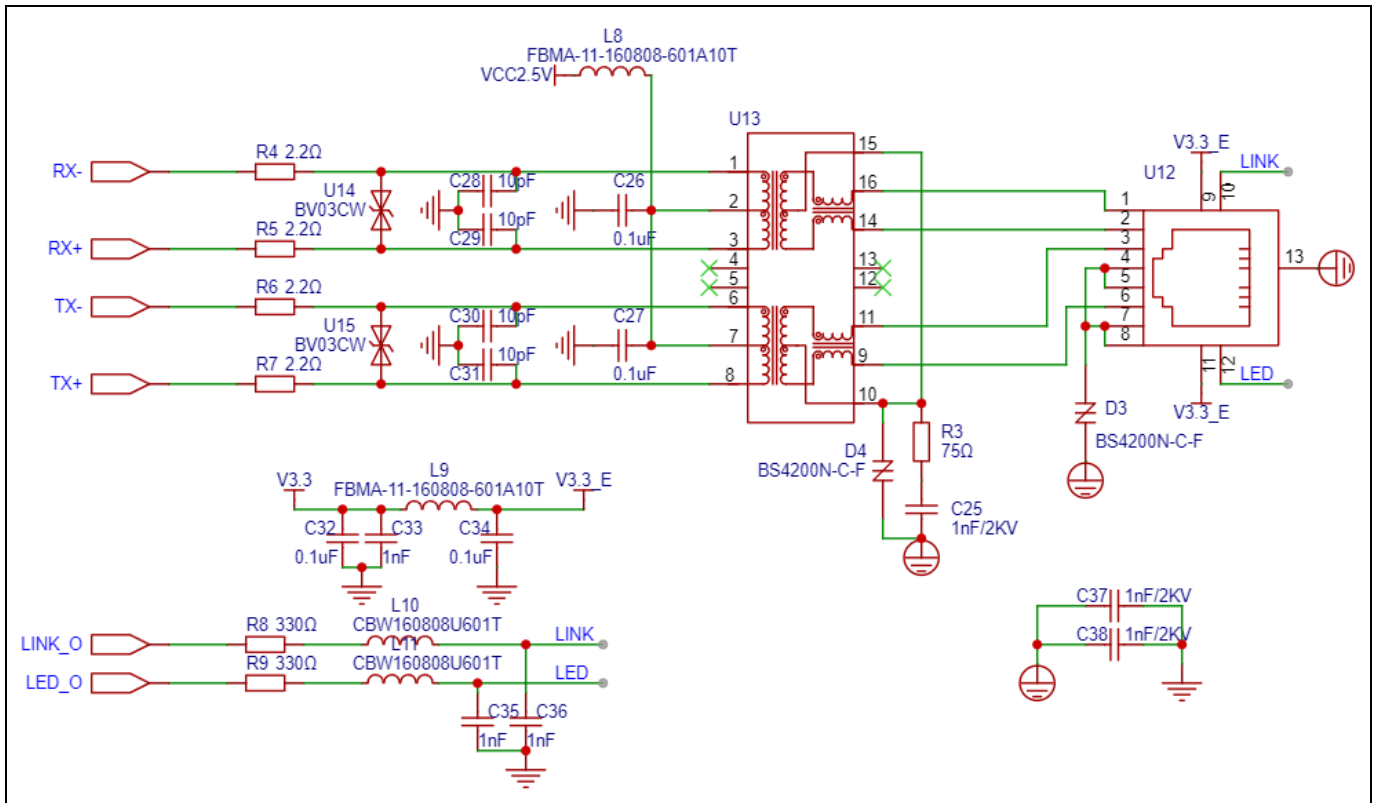
- C13/C14 are adjustable according to test results, less than 10 pF is recommended
- PGND is connected to GND if the product is made without metal chassis
- Optional array type TVS

Figure 36. RS232 interface



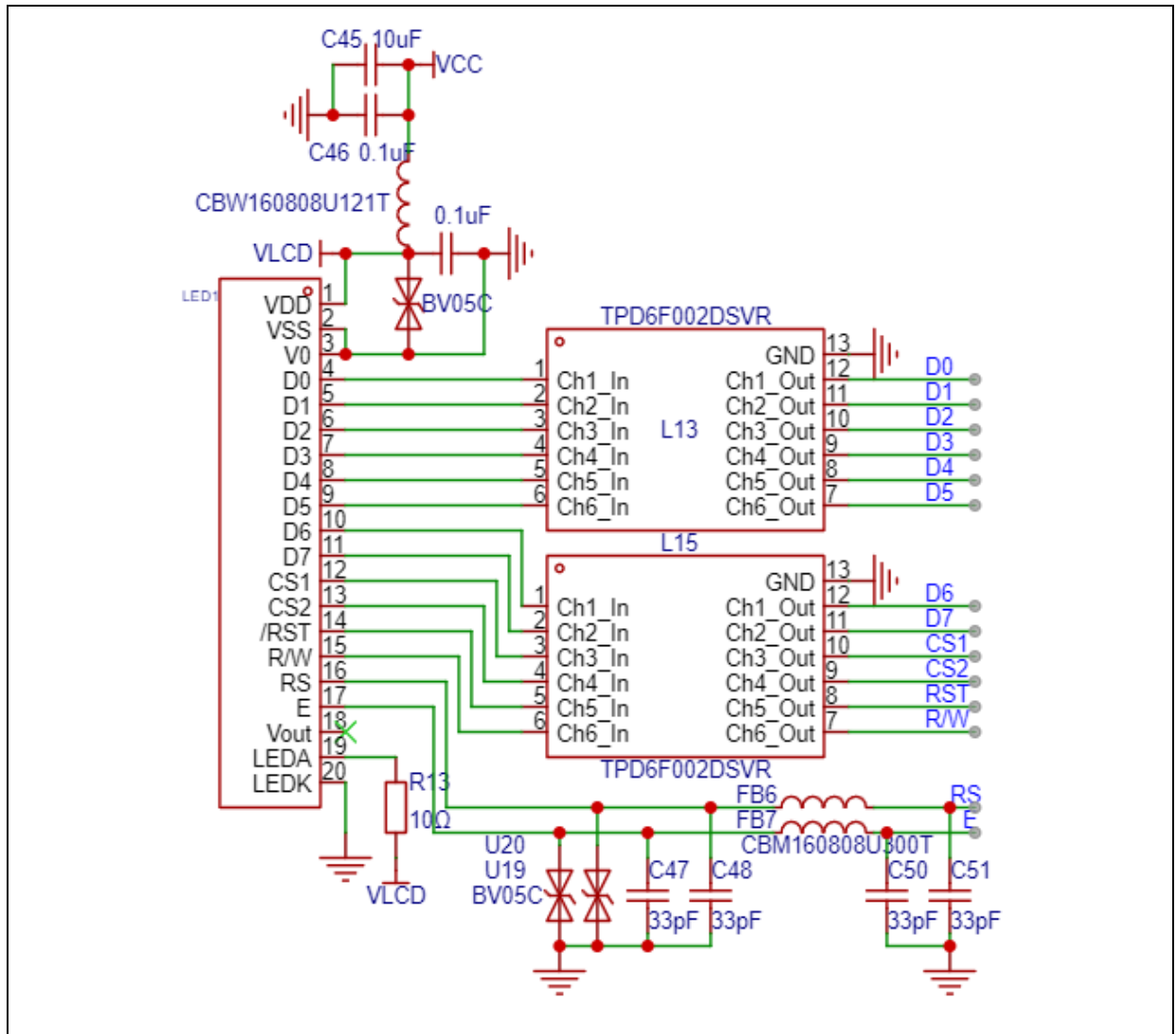
- R1/R2 are adjustable according to the actual needs
- TVS (U10/U11) and C18/C19 are connected to the chassis earth and placed close to the external connectors

Figure 37. 10/100M Ethernet interface



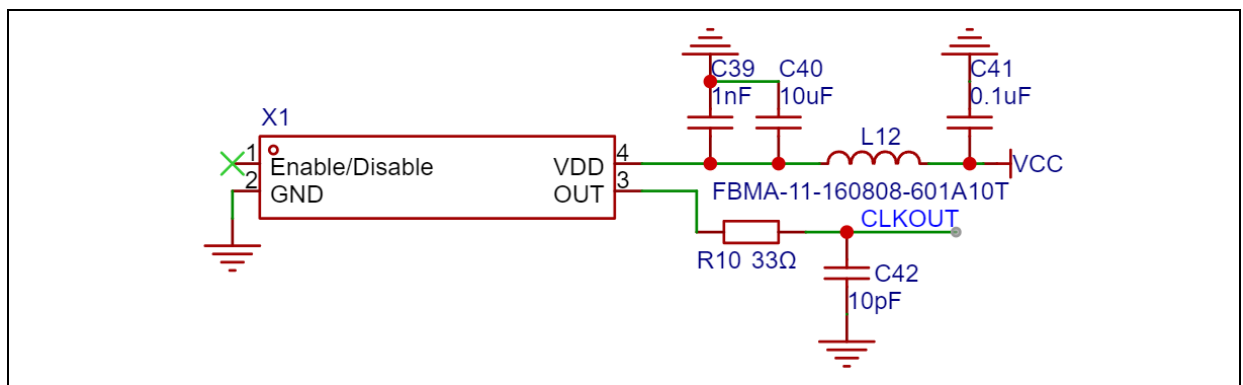
- C28/C29/C30/C31 are designed for future use
- The differential pair signal lines are routed in the same way as much as possible, and kept 3W away from other signals

Figure 38. LCD interface



- TPD6F002DSVR is an EMI filter with ESD protection
- TVS and filters are placed close to the connector
- LCD cable can be covered with a shielding according to the actual needs

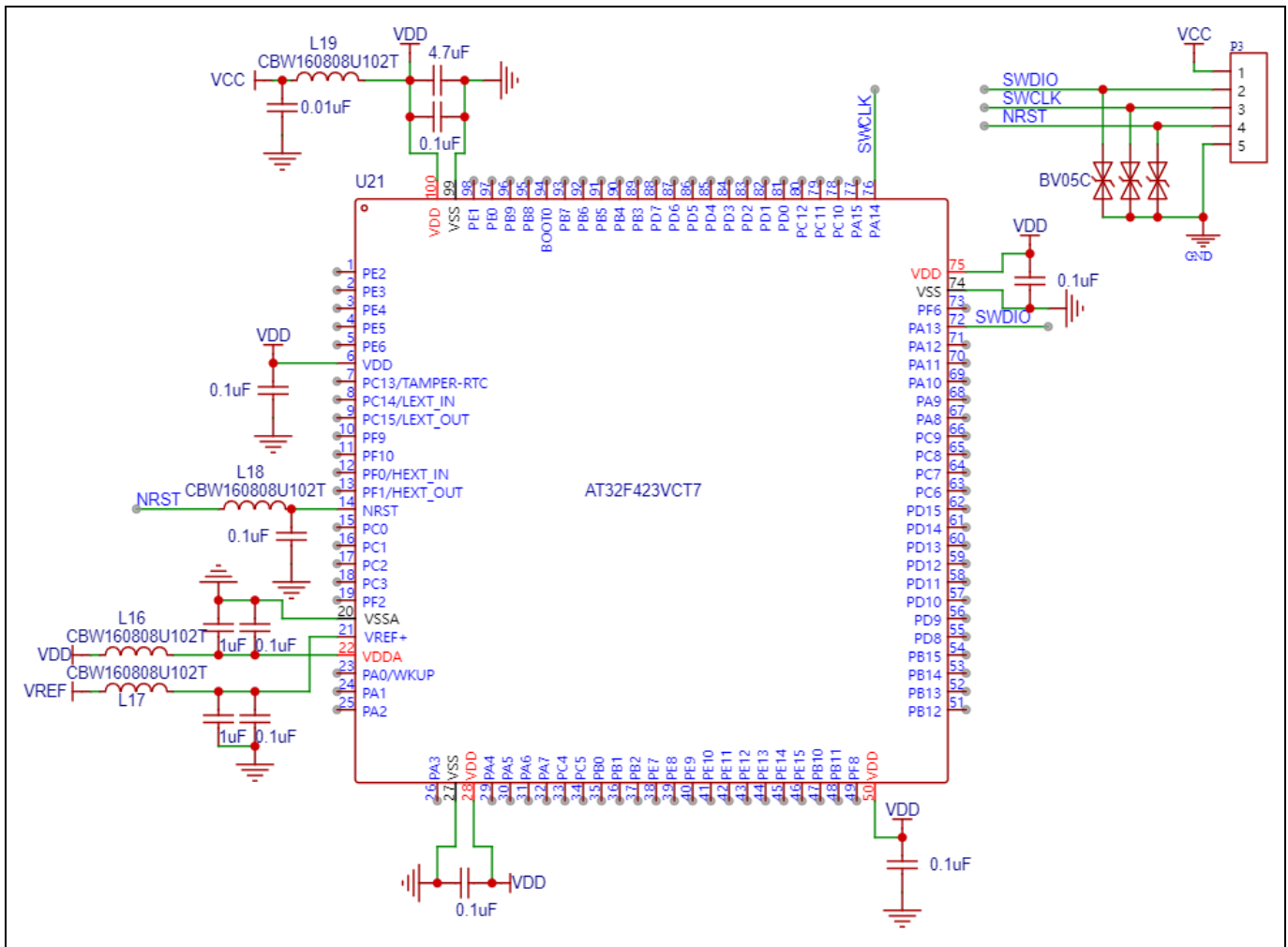
Figure 39. Oscillator



- R10/C42 are designed for future use and adjustable according to the actual needs

10.4 EMC design example for microcontroller

Figure 40. MCU



- All V_{SS}/V_{SSA} and bypass capacitors should be directly connected to the ground plane, not through ground wire
- Bypass capacitors should be placed as close to the pins as possible
- For other precautions on design, please refer to Chapter 7 through Chapter 9

11 Typical faults

This chapter describes some typical faults which may occur during the use of microcontrollers, with the aim of helping users identify real causes as soon as possible.

11.1 V_{DD} and V_{SS} short issue during product use or aging

Symptoms: system failed, MCU is abnormally hot, MCU power consumption goes up, V_{DD} and V_{SS} short (multimeter test)

Checklist:

- Is the V_{DD} voltage near or above upper limit?
- Is the V_{DD} overshoot and out of upper limit at the moment of system startup?
- Is the inductive load (electric relay or motor) generating voltage or current?
- Is MCU damaged by electrostatic charge?

11.2 GPIO damage during product use or aging

Symptoms: MCU is abnormally hot, MCU power consumption goes up, short between GPIO pins and V_{DD}/V_{SS} or GPIO unable to output high/low level (multimeter test)

Checklist:

- Is GPIO input voltage or pull-up voltage out of GPIO threshold?
- Is the V_{DD} overshoot and out of upper limit at the moment of system startup?
- Is the inductive load (electric relay or motor) generating transient voltage or current?
- Product test process flaw. For example, overlap circuit boards during testing, on-board high voltage energy-storage capacitor is shorted to GPIO when it is not fully discharged?
- Is GPIO damaged by electrostatic charge damage?

11.3 Crystal unable to vibrate or frequency output failure

Symptoms: the oscilloscope tested that there is no waveform output or output frequency failure on external crystal pins. After code debugging, it is found that STBL flag bit is not set.

Checklist:

- If passive crystal, is the accompanying/matching capacitor within spec? If active crystal, is the operating voltage within spec?
- Is the crystal route too long? Is there too much cross-layer routing? Is it receiving disturbance from high frequency circuits?
- Is the crystal frequency out of MCU spec?
- Is there any unsoldering issue on crystal? Is there any soldering residue surrounding routes?
- Does the software enable HEXTEN/LEXTEN? Is the STBL timeout settings too short?

11.4 ADC sampling data error

Checklist:

- Is V_{DDA}/V_{REF+} power supply being disturbed?
- Is the signal input impedance too large? Is there enough sampling time?
- Is the ADC clock and sampling rate set properly?
- Check software code configuration. Is there any out-of-order issue caused by DMA?
- Is the ADC_IN out of $V_{DD} + 0.3\text{ V}$?
- Are the sources of signals disturbed?
- Does the software have appropriate filtering algorithm?

12 Revision history

Table 4. Document revision history

Date	Revision	Changes
2021.5.5	1.0.0	Initial release
2021.12.22	1.0.1	Added ESD protection description
2022.2.25	2.0.0	1. Corrected descriptions of PVM-related registers 2. Added descriptions of conditions HEXT should be used in section 2.1
2022.5.13	2.0.1	Added section 7.2 QFN packages EPAD design tips
2022.11.29	2.0.2	Added sections 8.2.3 and 9.3.3 about software setting for noise immunity
2023.5.2	2.0.3	1. Added the descriptions of HEXT drive level in 2.1 2. Added the descriptions of USART/UART hardware in 7.1.3
2023.10.23	2.1.0	Added Chapter 10 EMC typical hardware design

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