ES0008
Errata sheet

AT32L021 device limitations

Chip identification

This errata sheet applies to the AT32L021 series. This series features an ARM™ 32-bit Cortex®-M0+ core.

Table 1. Device summary

Device	Flash memory	Part numbers
AT32L021	64 KB	AT32L021C8T7, AT32L021K8T7, AT32L021K8U7 AT32L021K8U7-4, AT32L021G8U7, AT32L021F8U7, AT32L021F8P7
	32 KB	AT32L021C6T7, AT32L021K6T7, AT32L021K6U7, AT32L021K6U7-4, AT32L021G6U7, AT32L021F6U7, AT32L021F6P7
	16 KB	AT32L021C4T7, AT32L021K4T7, AT32L021K4U7, AT32L021K4U7-4, AT32L021G4U7, AT32L021F4U7, AT32L021F4P7

Contents

List of tables

1 AT32L021 limitations

Table 2 summarizes the limitations on AT32A403A device that have been identified so far.

Table 2. Summary of device limitations

Sections	Description
1.1 TMR	1.1.1 Brake input failed when TMREN=0 (TMR disabled)
1.2 PWC	1.2.1 Unable to wake up Standby mode when Standby mode wakeup pin is active high
	1.2.2 POR/LVR with no Hysteresis
1.3 I2S	1.3.1 Data reception error when I2S 24-bit data is packed into 32-bit format
	1.3.2 First data error in I2S PCM standard long frame receive-only mode

1.1 TMR

1.1.1 Brake input failed when TMREN=0 (TMR disabled)

- Description:

  When TMREN=0 (Timer is not enabled), brake input failed to work, making it unable to trigger brake event or interrupt.

  Example: In single-cycle mode, TMREN is automatically cleared at the end of the one counting period. However due to aforementioned brake input failure, the output enable bit (OEN) cannot be cleared, and brake flag cannot be set either.

- Workaround:

  None.

- Revision history:

  None.

1.2 PWC

1.2.1 Unable to wake up Standby mode when Standby mode wakeup pin is active high

- Description:

  When the Standby mode wakeup pin is kept at high level, enabling the Standby mode wakeup pin cannot wake up MCU from Standby mode on a periodical basis. In this scenario, the possible result is that when the Standby mode wakeup pin remains high active, the MCU will enter Standby mode and wait for being woke up on a rising edge event.

- Workaround:

  First disable the Standby mode wakeup pin before enabling it later.

- Revision history:

  None.

1.2.2 POR/LVR with no Hysteresis

- Description:

  One of the characteristics with POR/LVR is that it has no Hysteresis or its Hysteresis is smaller than 20 mV. As a result, when the POR/LVR runs below 30 ms/V, the MCU is likely to be repeatedly started and reset. As the disturbance from V_{DD} gets stronger and the POR/LVR operates more slowly, the MCU getting started and then reset back and forth becomes more frequent.

- Workaround:

  It is recommended that based on the features of power supply used, the users insert appropriate delay before the GPIO operation command during the startup phase of code, in order to avoid this problem.

- Revision history:

  None.

1.3 I2S

1.3.1 Data reception error when I2S 24-bit data is packed into 32-bit format

- Description:

  For I²S, When 24-bit data are packed into 32-bit frame format, the remaining 8 invalid CLK data would be received as normal data by the receiver.

- Workaround:

  Method 1: Both the receiver and transmitter use the same way of packing 24-bit data into 32-bit format.
  Method 2: Discard these 8 invalid CLK data in the frame format using software.

- Revision history:

  None.

1.3.2 First data error in I2S PCM standard long frame receive-only mode

- Description:

  When the following three conditions are present for I²S, it is likely that the first data you receive is incorrect but the subsequent data can return to normal

  The three conditions are as follows:

  1. Set PCM long frame standard receive-only mode
  2. I2SCPOL = 0
  3. SCK remains high, which is abnormal, before I²S is enabled

- Workaround:

  Pull up or pull down the SCK pin externally or internally, depending on the I2SCLKPOL configuration.

- Revision:
  None.

2 Document revision history

Table 3. Document revision history

Date	Version	Changes
2024.01.11	2.0.0	Initial release

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Purchasers are solely responsible for the selection and use of ARTERY's products and services, and ARTERY assumes no liability whatsoever relating to the choice, selection or use of the ARTERY products and services described herein

No license, express or implied, to any intellectual property rights is granted under this document. If any part of this document deals with any third party products or services, it shall not be deemed a license granted by ARTERY for the use of such third party products or services, or any intellectual property contained therein, or considered as a warranty regarding the use in any manner of such third party products or services or any intellectual property contained therein.

Unless otherwise specified in ARTERY's terms and conditions of sale, ARTERY provides no warranties, express or implied, regarding the use and/or sale of ARTERY products, including but not limited to any implied warranties of merchantability, fitness for a particular purpose (and their equivalents under the laws of any jurisdiction), or infringement on any patent, copyright or other intellectual property right.

Purchasers hereby agree that ARTERY's products are not designed or authorized for use in: (A) any application with special requirements of safety such as life support and active implantable device, or system with functional safety requirements; (B) any aircraft application; (C) any aerospace application or environment; (D) any weapon application, and/or (E) or other uses where the failure of the device or product could result in personal injury, death, property damage. Purchasers' unauthorized use of them in the aforementioned applications, even if with a written notice, is solely at purchasers' risk, and Purchasers are solely responsible for meeting all legal and regulatory requirements in such use.

Resale of ARTERY products with provisions different from the statements and/or technical characteristics stated in this document shall immediately void any warranty grant by ARTERY for ARTERY's products or services described herein and shall not create or expand any liability of ARTERY in any manner whatsoever.