ES0010
Errata Sheet

AT32F423 device limitations

Device identification

This errata sheet applies to ARTERY AT32F423 microcontrollers based on an ARM™ 32-bit Cortex®-M4 core.

Table 1. Device summary

Device	Flash memory	Part number
AT32F423	256 KB	AT32F423VCT7，AT32F423RCT7，AT32F423RCT7-7，AT32F423CCT7，AT32F423CCU7，AT32F423TCU7，AT32F423KCU7-4
	128 KB	AT32F423VBT7，AT32F423RBT7，AT32F423RBT7-7，AT32F423CBT7，AT32F423CBU7，AT32F423TBU7，AT32F423KBU7-4
	64 KB	AT32F423V8T7，AT32F423R8T7，AT32F423R8T7-7，AT32F423C8T7，AT32F423C8U7，AT32F423T8U7，AT32F423K8U7-4

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Table 2. Summary of device limitations

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1.1 GPIO

1.1.1 PC13-related features unavailable during slower MCU power-on

- Description:

  In the process of MCU being powered on at a slower rate, there is a possibility that PC13-related functions such as input/output, ERTC tamper detection are unavailable.

- Workaround:

  Perform another system reset following this power on. See the reference code below:

```
if((CRM->ctrlsts_bit.porrstf == SET) && (CRM->ctrlsts_bit.swrstf == RESET))
{
  NVIC_SystemReset();
}
```

  After above operation, software reset flag (SWRSTF) will be set. If the application program needs to perform corresponding operations based on SWRSTF bit, follow the procedures below:

  A. When the software reset flag and power-on reset flag are set simultaneously, it means that this is a system reset used to solve PC13 issues. Thus there is a need to clear all reset flags by calling relevant functions.

  B. When the software reset flag is set but power-on reset flag isn't set, it indicates that this is a system reset performed by the program application layer for application processing.

1.2 I2C

1.2.1 Digital filtering function disabled in slave mode

- Description:

  In I2C slave mode, digital filtering function is disabled, making it unable to filter disturbance.

- Workaround:

  None.

1.3 I2S

1.3.1 UDR flag is set in I2S slave transmit mode and discontinuous communication state

- Description:

  The UDR flag is still set in I2S slave transmit mode alongside discontinuous communication state, even if data have been written before the start of communication.

- Workaround:

  According to the protocols, it is recommended to use DMA or interrupts for fast data transfer in I2S slave transmit mode, in order to guarantee continuous communication.

1.3.2 Data reception error when 24-bit data is packed into 32-bit format

- Description:

  When 24-bit data is packed into a format of 32-bit frame, the remaining 8 invalid CLK data would be received by the receiver as normal data.

- Workaround:

  Method 1: Both the receiver and transmitter use the same way of packing 24-bit data into 32-bit format.
  Method 2: Discard these 8 invalid CLK data using software.

1.4 PWC

1.4.1 PVM event generated after PVM enable when VDD is above PVM threshold

- Description:

  Enabling PWC voltage monitoring feature when the VDD is greater than PVM threshold will immediately generate an unexpected PVM event.

- Workaround:

  Clear the unexpected PVM event during PVM initialization.

1.4.2 Unable to wakeup Deepsleep mode after AHB frequency division

- Description:

  After AHB frequency is divided, no wakeup sources can wake up Deepsleep mode.

- Workaround:

  Do not divide AHB frequency in Deepsleep mode.

  Remove AHB frequency division before entering Deepsleep mode. Configure then the desired AHB frequency after waking up Deepsleep mode.

1.4.3 Unable to enable HEXT after waking up Deepsleep mode

- Description:

  When the following three conditions are present for PWC, HEXT cannot be enabled after Deepsleep mode is woke up.
  The three conditions include:
  1. Set DBG_DEEPSLEEP = 1
  2. Attempt to wake up Deepsleep mode at the moment when the Deepsleep mode is being entered. In other words, a wakeup source arrives within three LICK cycles after Deepsleep mode entry command is executed
  3. Enable HEXT immediately after waking up Deepsleep mode

- Workaround:

  After waking up Deepsleep mode, wait around 3 LICK clock cycles before enabling HEXT.

1.4.4 Precautions on software accessing BPR registers

- Description:

  When the V_{DD} power-on rate is lower than 1.3 ms/V, operating battery-powered domain registers (BPR) through software may cause system exception until V_{DD} rises up to 2.57V.

  Battery-powered domain registers (BPR) include:

  A) All ERTC registers

  B) Battery-powered domain control register (CRM_BPDC)

  C) LICKEN and LICKSTBL bits in the CRM_CTRLSTS register

- Workaround:

  Insert a delay of 60ms with software after system reset to ensure that V_{DD} reaches 2.57V before accessing BPR registers, see code below for reference:

```
/**
  * @brief   take some delay for waiting power stable, delay is about 60ms with frequency 8MHz.
  * @param   none
  * @retval none
  */
void wait_for_power_stable(void)
{
  volatile uint32_t delay = 0;
  for(delay = 0; delay < 50000; delay++);
}

int main(void)
{
  /* add a necessary delay to ensure that Vdd is higher than the operating
      voltage of battery powered domain (2.57V) when the battery powered
      domain is powered on for the first time and being operated. */
  wait_for_power_stable();

  /* congfig the system clock */
  system_clock_config();

  /* config ertc or other operations of battery powered domain */
  ertc_config();
  while(1)
  {
  }
}
```

1.5 ERTC

1.5.1 Read/write ERTC occupies APB1 for 15 ERTC clock cycles

- Description:

  As reading/writing ERTC registers takes approximately 15 APB1 clock cycles to be synchronized with battery powered domain, APB1 is occupied and DMA transfer on APB1 also stops during this period. After the completion of synchronization, APB1 is released automatically, and also DMA transfer continues execution.

- Workaround:

  After ERTC initialization, users need minimize the times of writing ERTC registers provided that ERTC features can satisfy users' needs, in order to reduce its impact on system.

1.6 ADC

1.6.1 ADC unable to reach its maximum sampling rate

- Description:

  As its internal default setting values are inappropriate, ADC characteristics obviously deviate from its ideal values, thus resulting in such problems as missing codes and inaccuracy.

- Workaround:

  When ADC clock is ON but ADC and its calibration is yet to be enabled, first write 0x09 to the XTEST bit in the ADC_MSIC register before starting using ADC.

1.7 TMR

1.7.1 Break input failed when TMREN=0

- Description:

  When TMREN=0 (timer is disabled), break input is inactive, causint it unable to trigger break event or interrupt.
  As an example, in one-pulse mode, the TMREN is automatically cleared at the end of one-cycle counting. In such case, due to the break input being disabled, the output enable bit (OEN) cannot be cleared, nor is the break flag bit set.

- Workaround:

  None.

1.8 CAN

1.8.1 Fail to cancel mailbox transmit command when CAN bus disconnected

- Description:

  As a node for data transmission, if the following two conditions are both present for CAN, it is not possible to clear or cancel a transmit command in a mailbox within CAN error passive interrupt, causing that the to-be-sent message command has not been canceled during the period of CAN bus being disconnected, and such message would be retransmitted after CAN bus communication resumes.

  1. CAN bus (CANH/L) is disconnected intentially or accidentally
  2. Auotmaitc retransmission feature is enabled

- Workaround:

  When a message failed to be sent out for several times, disable automatic retransmission feature when the following two conditions are met at the same time:

  1. Error type is “Passive bit error”
  2. Mailbox transmit state is “mailbox_x transmit error”

  Then re-activate auto retransmission feature in the subsequent CAN message transmit function.

2 Document revision history

Table 3. Document revision history

Date	Revision	Changes
2023.01.09	2.0.0	Initial release
2023.08.03	2.0.1	1. Added *1.7.1 Break input failed when TMREN=0* 2. Added *1.8.1 Fail to cancel mailbox transmit command when CAN bus disconnected*
2023.08.18	2.0.2	Updated “Workaround” i*n 1.4.4 Precautions on software accessing BPR registers*

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