ES0011
Errata Sheet

AT32F402/405 device limitations

Device identification

This errata sheet applies to ARTERY AT32F402/405 microcontrollers which is based on an ARM® 32-bit Cortex®-M4 core.

Table 1. Device summary

Device	Flash memory	Part number
AT32F402/405	256 KB	AT32F405RCT7, AT32F405RCT7-7 AT32F405CCT7, AT32F405CCU7 AT32F405KCU7-4, AT32F402RCT7 AT32F402RCT7-7, AT32F402CCT7, AT32F402CCU7, AT32F402KCU7-4,
	128 KB	AT32F405RBT7, AT32F405RBT7-7, AT32F405CBT7, AT32F405CBU7, AT32F405KBU7-4, AT32F402RBT7, AT32F402RBT7-7, AT32F402CBT7, AT32F402CBU7, AT32F402KBU7-4,

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1 AT32F402/405 device limitations

Table 2 gives a list of limitations that have been identified so far on the AT32F402/405 devices.

Table 2. Summary of device limitations

Sections	Description
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1.2 ERTC	1.2.1 Read/write ERTC occupies APB1 for 15 ERTC clock cycles
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1.1 PWC

1.1.1 PVM event generated after PVM enable when VDD is above PVM threshold

- Description:

  Enabling PWC voltage monitoring feature while the VDD is greater than PVM threshold will trigger an unexpected PVM event.

- Workaround:

  Clear the unexpected PVM event during PVM initialization.

1.1.2 Unable to wakeup Deepsleep mode after AHB frequency division

- Description:

  After AHB frequency is divided, no wakeup sources can wake up Deepsleep mode.

- Workaround:

  Do not divide AHB frequency while using Deepsleep mode.

  Remove AHB frequency division before entering Deepsleep mode. Configure then the desired AHB frequency after waking up Deepsleep mode.

1.1.3 Higher power consumption in Deepsleep mode because of OTGHS PHY default setting

- Description:

  The device direct entry into Deepsleep mode may lead to power consumption of up to 3.5 mA.

- Workaround:

  Refer to PWC DEEPSLEEP DEMO to configure relevant registers.

  The demo is located at project\at_start_f402\examples\pwc\deepsleep_ertc_alarm

1.2 ERTC

1.2.1 Read/write ERTC occupies APB1 for 15 ERTC clock cycles

- Description:

  As reading/writing ERTC registers takes around 15 APB1 clock cycles to be synchronized with battery powered domain, APB1 is occupied and DMA transfer on APB1 also is halted during this period. After the completion of synchronization, APB1 is released automatically, and DMA transfer continues execution.

- Workaround:

  After ERTC initialization, users need minimize the times of writing ERTC registers provided that ERTC features can satisfy users' needs, in order to reduce its impact on system.

1.3 CRM

1.3.1 CRM_BPDC/CRM_CTRLSTS registers limitations

- Description:

  Accessing CRM_BPDC register and CRM_CTRLSTS register may not work when the AHB domain is greater than 120 MHz.

- Workaround:

  Accessing these registers is made possible when the AHB domain is no more than 120 MHz. This means that the maximum allowable frequency of the AHB domain while accessing these two registers is 120 MHz.

  See reference code below:

```
/**
  * @brief  main function.
  * @param  none
  * @retval none
  */
int main(void)
{
  /*access  the CRM_BPDC/CRM_CTRLSTS register here*/
  crm_ertc_clock_enable(TRUE) ;

  system_clock_config();
  …
  while(1)
  {
    …
  }
}
```

1.4 QSPI

1.4.1 DMA P2M mode usage condition in QSPI command port mode

- Description:

  When QSPI is configured in command port mode, a specific condition must be respected to use DMA P2M mode for data transfer, detailed as follows.

- Workaround:

  When QSPI is configured in command port mode, to use DMA P2M mode to transfer data, the MSIZE must select word format, and data size must be a multiple of 4.

1.4.2 Excess dummy clock sent after read operation in QSPI command port mode

- Description:

  When QSPI is configured in command port mode, after the completion of read access, an additional dummy clock will be sent, which has no impact on applications in most cases.

- Workaround:

  None.

1.5 GPIO

1.5.1 PC13-related features unavailable during slower MCU power-on

- Description:

  In the process of MCU being powered on at a slower rate, there is a possibility that PC13-related functions such as input/output, ERTC tamper detection are unavailable.

- Workaround:

  Perform another system reset following this power on. See the reference code below:

```
if((CRM->ctrlsts_bit.porrstf == SET) && (CRM->ctrlsts_bit.swrstf == RESET))
{
  NVIC_SystemReset();
}
```

  After above operation, software reset flag (SWRSTF) will be set. If the application program needs to perform corresponding operations based on SWRSTF bit, follow the procedures below:

  A. When the software reset flag and power-on reset flag are set simultaneously, it means that this is a system reset used to solve PC13 issues. Thus there is a need to clear all reset flags by calling relevant functions.

  B. When the software reset flag is set but power-on reset flag isn't, it indicates that this is a system reset performed by the program application layer for application processing.

1.6 CAN

1.6.1 Fail to cancel mailbox transmit command when CAN bus disconnected

- Description:

  As a node for data transmission, if the following two conditions are both present for CAN, it is not possible to clear or cancel a transmit command in a mailbox within CAN error passive interrupt, causing that the to-be-sent message command has not been canceled during the period of CAN bus being disconnected, and such message would be retransmitted after CAN bus communication resumes.

  The two conditions include:

  1. CAN bus (CANH/L) is disconnected intentionally or accidentally
  2. Automatic retransmission feature is enabled

- Workaround:

  When a message failed to be sent out for several times, disable automatic retransmission feature when the following two conditions are met at the same time:

  1. Error type is “Passive bit error”
  2. Mailbox transmit state is “mailbox_x transmit error”

  Then re-activate auto retransmission feature in the subsequent CAN message transmit function.

2 Document revision history

Table 3. Document revision history

Date	Revision	Changes
2023.08.03	2.0.0	Initial release

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