

AT32A423 device limitations

Device identification

This errata sheet applies to ARTERY AT32A423 microcontrollers based on an ARM™ 32-bit Cortex®-M4 core.

Table 1. Device summary

Device	Flash memory	Part number
AT32A423	256 KB	AT32A423VCT7, AT32A423RCT7, AT32A423RCT7-7, AT32A423CCT7, AT32A423CCU7, AT32A423TCU7, AT32A423KCU7-4
	128 KB	AT32A423VBT7, AT32A423RBT7, AT32A423RBT7-7, AT32A423CBT7, AT32A423CBU7, AT32A423TBU7, AT32A423KBU7-4
	64 KB	AT32A423V8T7, AT32A423R8T7, AT32A423R8T7-7, AT32A423C8T7, AT32A423C8U7, AT32A423T8U7, AT32A423K8U7-4

Contents

1	AT32A423 device limitations	4
1.1	GPIO	5
1.1.1	PC13 function unavailable during slower MCU power-on	5
1.2	I2C.....	5
1.2.1	Digital filtering function disabled in slave mode	5
1.3	I2S.....	5
1.3.1	UDR flag is set in I2S slave transmit mode with discontinuous communication state	5
1.3.2	Data reception error when 24-bit data is packed into 32-bit format.....	6
1.4	PWC.....	6
1.4.1	PVM event generated after PVM enabled when VDD above PVM threshold	6
1.4.2	Unable to wakeup Deepsleep mode after AHB frequency division	6
1.4.3	Unable to enable HEXT after waking up Deepsleep mode	6
1.4.4	Precautions on software accessing BPR registers.....	7
1.5	ERTC	8
1.5.1	Read/write ERTC occupies APB1 for 15 ERTC clock cycles	8
1.6	ADC.....	8
1.6.1	ADC unable to reach its maximum sampling rate.....	8
1.7	TMR	8
1.7.1	Break input failed when TMREN=0.....	8
1.8	CAN.....	9
1.8.1	Fail to cancel mailbox transmit command when CAN bus disconnected.....	9
2	Document revision history	10

List of tables

Table 1. Device summary	1
Table 2. Summary of device limitations	4
Table 3. Document revision history.....	10

1 AT32A423 device limitations

Table 2 gives a list of limitations that have been identified so far on the AT32A423 devices.

Table 2. Summary of device limitations

Sections	Description
GPIO	1.1.1 PC13 function unavailable during slower MCU power-on
I2C	1.2.1 Digital filtering function disabled in slave mode
I2S	1.3.1 UDR flag is set in I2S slave transmit mode with discontinuous communication state
	1.3.2 Data reception error when 24-bit data is packed into 32-bit format
PWC	1.4.1 PVM event generated after PVM enabled when VDD above PVM threshold
	1.4.2 Unable to wakeup Deepsleep mode after AHB frequency division
	1.4.3 Unable to enable HEXT after waking up Deepsleep mode
	1.4.4 Precautions on software accessing BPR registers
ERTC	1.5.1 Read/write ERTC occupies APB1 for 15 ERTC clock cycles
ADC	1.6.1 ADC unable to reach its maximum sampling rate
TMR	1.7.1 Break input failed when TMREN=0
CAN	1.8.1 Fail to cancel mailbox transmit command when CAN bus disconnected

1.1 GPIO

1.1.1 PC13 function unavailable during slower MCU power-on

- Description:

In the process of MCU being powered on at a slower rate, there is a possibility that PC13-related functions (such as input/output, ERTC tamper detection) are unavailable.

- Workaround:

Perform another system reset following this power on. See the reference code below:

```
if((CRM->ctrists_bit.porrstf == SET) && (CRM->ctrists_bit.swrstf == RESET))
{
    NVIC_SystemReset();
}
```

After above operation, software reset flag (SWRSTF) will be set. Then the application can use code to determine what the software reset flag really means.

- A. When the software reset flag and power-on reset flag are set simultaneously, it means that this is a system reset used to solve PC13 issues. Thus there is a need to clear all reset flags by calling relevant functions.
- B. When the software reset flag is set but power-on reset flag isn't set, it indicates that this is a system reset performed by the program application layer.

1.2 I2C

1.2.1 Digital filtering function disabled in slave mode

- Description:

In I2C slave mode, digital filtering function is deactivated, making it unable to filter disturbance.

- Workaround:

None.

1.3 I2S

1.3.1 UDR flag is set in I2S slave transmit mode with discontinuous communication state

- Description:

The UDR flag is still set in I2S slave transmit mode alongside discontinuous communication state, even if data have been written before the start of communication.

- Workaround:

According to the protocol, it is recommended to use DMA or interrupts for fast data transfer in I2S slave transmit mode, in order to guarantee continuous communication.

1.3.2 Data reception error when 24-bit data is packed into 32-bit format

- Description:
When 24-bit data is packed into a 32-bit frame format, the remaining 8 invalid CLK data would be received by the receiver as normal data.
- Workaround:
Method 1: Both the receiver and transmitter use the same way of packing 24-bit data into 32-bit format.
Method 2: Discard these 8 invalid CLK data using software.

1.4 PWC

1.4.1 PVM event generated after PVM enabled when VDD above PVM threshold

- Description:
Enabling PWC voltage monitoring feature when the VDD is greater than PVM threshold will immediately generate an unexpected PVM event.
- Workaround:
Clear the unexpected PVM event during PVM initialization.

1.4.2 Unable to wakeup Deepsleep mode after AHB frequency division

- Description:
After AHB frequency is divided, no wakeup sources can wake up Deepsleep mode.
- Workaround:
Do not divide AHB frequency in Deepsleep mode.
Remove AHB frequency division before entering Deepsleep mode. Then set the desired AHB frequency after waking up Deepsleep mode.

1.4.3 Unable to enable HEXT after waking up Deepsleep mode

- Description:
When the following three conditions are present for PWC, HEXT cannot be enabled after Deepsleep mode is woke up.
The three conditions include:
 1. Set `DBG_DEEPSLEEP = 1`
 2. Wake up Deepsleep mode at the moment the Deepsleep mode is being entered. In other words, a wakeup source arrives within three LICK cycles of Deepsleep mode entry command being executed
 3. Enable HEXT immediately after waking up Deepsleep mode
- Workaround:
After waking up Deepsleep mode, wait around 3 LICK clock cycles before enabling HEXT.

1.4.4 Precautions on software accessing BPR registers

- Description:

When the V_{DD} power-on rate is lower than 1.3 ms/V, operating battery-powered domain registers (BPR) through software may result in system exception until V_{DD} rises up to 2.57V.

Battery-powered domain registers (BPR) include:

- A) All ERTC registers
- B) Battery-powered domain control register (CRM_BPDC)
- C) LICKEN and LICKSTBL bits in the CRM_CTRLSTS register

- Workaround:

Insert a delay of 60ms with software after system reset to make sure that V_{DD} reaches 2.57V before accessing BPR registers, see code below for reference:

```
/**
 * @brief take some delay for waiting power stable, delay is about 60ms with frequency 8MHz.
 * @param none
 * @retval none
 */
void wait_for_power_stable(void)
{
    volatile uint32_t delay = 0;
    for(delay = 0; delay < 50000; delay++);
}

int main(void)
{
    /* add a necessary delay to ensure that Vdd is higher than the operating
       voltage of battery powered domain (2.57V) when the battery powered
       domain is powered on for the first time and being operated. */
    wait_for_power_stable();

    /* config the system clock */
    system_clock_config();

    /* config ertc or other operations of battery powered domain */
    ertc_config();
    while(1)
    {
    }
}
```

1.5 ERTC

1.5.1 Read/write ERTC occupies APB1 for 15 ERTC clock cycles

- Description:

As reading/writing ERTC registers takes approximately 15 APB1 clock cycles to synchronize with battery powered domain, APB1 is occupied and DMA transfer on APB1 also stops during this period. After the completion of synchronization, APB1 is released automatically, and also DMA transfer continues.

- Workaround:

After ERTC initialization, users need minimize the times of writing ERTC registers provided that ERTC features can satisfy users' needs, in order to reduce its impact on system.

1.6 ADC

1.6.1 ADC unable to reach its maximum sampling rate

- Description:

As its internal default setting values are inappropriate, ADC characteristics obviously deviate from its ideal values, thus resulting in such problems as missing codes and inaccuracy.

- Workaround:

When ADC clock is ON but ADC and its calibration is yet to be enabled, it is necessary to first write 0x09 to the XTEST bit in the ADC_MSIC register before starting using ADC.

1.7 TMR

1.7.1 Break input failed when TMREN=0

- Description:

When TMREN=0 (timer is disabled), break input is inactive, causing it unable to trigger break event or interrupt.

For example, in one-pulse mode, the TMREN is automatically cleared at the end of one-cycle counting. In such case, due to the break input being disabled, the output enable bit (OEN) cannot be cleared, nor is the break flag bit set.

- Workaround:

None.

1.8 CAN

1.8.1 Fail to cancel mailbox transmit command when CAN bus disconnected

- Description:

As a node for data transmission, if the following two conditions are both met for CAN, it is impossible to clear or cancel a transmit command in a mailbox within CAN error passive interrupt, so that the to-be-sent message command has not been canceled during the period of CAN bus being disconnected, and such message would be retransmitted after CAN bus communication resumes.

1. CAN bus (CANH/L) is disconnected intentionally or accidentally
2. Automatic retransmission feature is enabled

- Workaround:

When a message failed to be sent out for several times, the automatic retransmission feature should be enabled when the following two conditions are both met:

1. Error type is "Passive bit error"
2. Mailbox transmit state is "mailbox_x transmit error"

Then re-activate auto retransmission feature in the subsequent CAN message transmit function.

2 Document revision history

Table 3. Document revision history

Date	Revision	Changes
2024.03.06	2.0.0	Initial release

IMPORTANT NOTICE – PLEASE READ CAREFULLY

Purchasers are solely responsible for the selection and use of ARTERY's products and services, and ARTERY assumes no liability whatsoever relating to the choice, selection or use of the ARTERY products and services described herein

No license, express or implied, to any intellectual property rights is granted under this document. If any part of this document deals with any third party products or services, it shall not be deemed a license granted by ARTERY for the use of such third party products or services, or any intellectual property contained therein, or considered as a warranty regarding the use in any manner of such third party products or services or any intellectual property contained therein.

Unless otherwise specified in ARTERY's terms and conditions of sale, ARTERY provides no warranties, express or implied, regarding the use and/or sale of ARTERY products, including but not limited to any implied warranties of merchantability, fitness for a particular purpose (and their equivalents under the laws of any jurisdiction), or infringement on any patent, copyright or other intellectual property right.

Purchasers hereby agree that ARTERY's products are not designed or authorized for use in: (A) any application with special requirements of safety such as life support and active implantable device, or system with functional safety requirements; (B) any aircraft application; (C) any aerospace application or environment; (D) any weapon application, and/or (E) or other uses where the failure of the device or product could result in personal injury, death, property damage. Purchasers' unauthorized use of them in the aforementioned applications, even if with a written notice, is solely at purchasers' risk, and Purchasers are solely responsible for meeting all legal and regulatory requirements in such use.

Resale of ARTERY products with provisions different from the statements and/or technical characteristics stated in this document shall immediately void any warranty grant by ARTERY for ARTERY's products or services described herein and shall not create or expand any liability of ARTERY in any manner whatsoever.

© 2024 Artery Technology -All rights reserved