SC0073
Sample Code

How to connect AT32F407/437 EMAC to various PHY

Introduction

This sample code is written to demonstrate how to connect AT32F407/437 EMAC to different PHY and corresponding configuration.

EMAC supports MII mode and RMII mode, which can be selected through code configuration. When selecting, users also need to select corresponding RMII or MII mode on PHY evaluation board. For some products, their PHY supports only RMII or MII, which should be selected according to PHY files.

For PHY schematic, please refer to Ethernet TEST BOARD.

Applicable products:

Product series	AT32F407xx
	AT32F437xx

List of major peripherals used:

Peripherals	EMAC

List of PHY supported:

PHY	DM9162
	DP83848C
	LAN8720A
	AR8032
	IP101GR
	RTL8201F
	YT8512
	IP175LL
	IP179N

1 Quick start

1.1 Hardware resources

1) Ethernet Main Board (AT32F407/AT32F437)
2) Ethernet Sub board (DM9162, DP83848C, LAN8720A, LAN8720A…)
3) Connect Main Board to Sub board
4) Select corresponding MII or RMII mode
5) Select corresponding clock sources (it is advised to use a crystal to clock PHY since PLL clock output by MCO may not be able to meet PHY requirements)

Note 1: LAN8720A supports RMII mode only.

Note 2: For DP83848, in RMII mode, it is recommended to provide 50MHz crystal to PHY. Do not use PLL to output 50MH to PHY.

Note 3: At present, AR8032 only supports MII mode.

1.2 Software resources

There wer demos:

- at32f407_emac_phy_demo (AT32F407 EMAC Demo)
- at32f437_emac_phy_demo (AT32F437 EMAC Demo)

1.3 Example case

Through software:

Open the corresponding emac_phy_demo (project\at_start_f4xx\examples\emac\emac_phy_demo)

- *In* at32_emac.h, select corresponding PHY and MII or RMII mode

```
/* Select PHY MII or RMII Mode */
//#define MII_MODE
#define RMII_MODE


/* DM9162 Support RMII and MII */
#define DM9162


/* DP83848 Support RMII and MII, RMII Must CLK_OUT 50MHz Clock */
//#define DP83848


/* LAN8720 Support just only support RMII */
//#define LAN8720


/* RTL8201F Support RMII and MII */
//#define RTL8201F
```

```
/* AR8032 Support MII */
//#define AR8032

/* YT8512 Support RMII and MII */
//#define YT8512

/* IP101GR Support RMII and MII */
//#define IP101GR
//#define IP179N

#define IP175LLF
```

- Compile and download to main board
- Connect the internet cable, and use PC to ping 192.168.81.37 to test if internect connection is successful
- Call *ethernetif_set_link* to proceed with LWIP of internet connection status

```
#if (LINK_DETECTION > 0)
  /* link detection process every 500 ms */
  if (localtime - link_timer >= 500)
  {
    link_timer =  localtime;
    ethernetif_set_link(&netif);
  }
#endif

void ethernetif_set_link(void const *argument)
{
  uint16_t regvalue = 0;
  struct netif *netif = (struct netif *)argument;

  /* read phy_bsr*/
  regvalue = link_update();

  if(regvalue > 0)
  {
    at32_led_on(LED4);
    at32_led_off(LED2);
```

```
    }
    else
    {
      at32_led_on(LED2);
      at32_led_off(LED4);
    }
    /* check whether the netif link down and the phy link is up */
    if(!netif_is_link_up(netif) && (regvalue))
    {
      /* network cable is connected */
      netif_set_link_up(netif);
    }
    else if(netif_is_link_up(netif) && (!regvalue))
    {
      /* network cable is dis-connected */
      netif_set_link_down(netif);
    }
}
```

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
2021.11.10	2.0.0	Initial release
2022.04.26	2.0.1	Added internet connection status detection function
2022.11.18	2.0.2	Updated the description with regard to PHY clock source
2022.12.29	2.0.3	Added PHY IP175LL and IP179N support

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