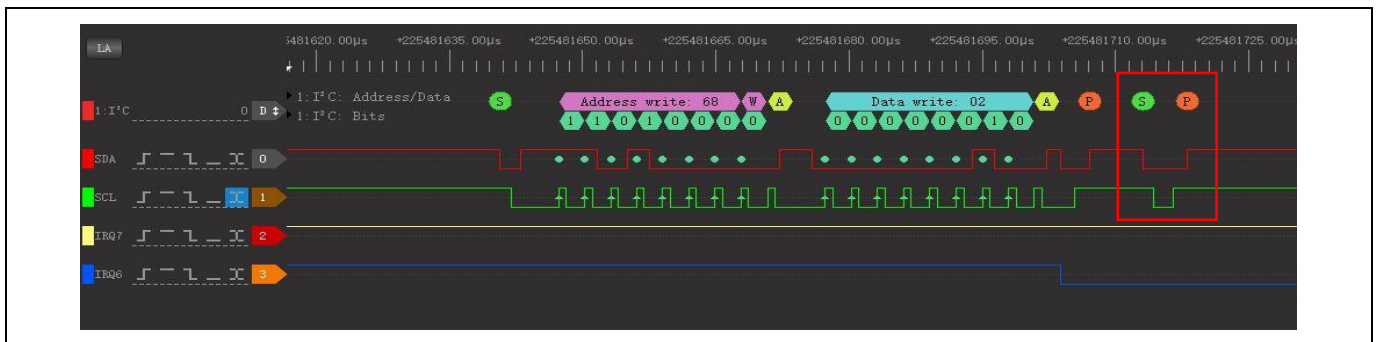


Unexpected STOP generation while writing data in I2C master mode

Questions:

In I2C master mode and after address is sent, an unexpected STOP is generated while writing data (master-transmit mode)



Answer:

The GENSTOP bit of the I2C_CTRL1 register is described as follows:

Bit 9	GENSTOP	0x0	rw	<p>Generate stop condition</p> <p>This bit is set or cleared by software. It is cleared when a Stop condition is detected. It is set by hardware when a timeout error is detected.</p> <p>0: No Stop condition is generated.</p> <p>1: Stop condition is generate.</p> <p>The salve releases the SCL and SDA lines when this bit is set in slave mode.</p>
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After sending STOP by setting the GENSTOP bit of the I2C_CTRL register, this bit shall be cleared by hardware before starting next operation (such as, set GENSTART at the start of the next communication) in the I2C_CTRL1 register. If this step is skipped (that is, the GENSTOP bit is not cleared by hardware before executing other operation), hardware logic fault may occur, resulting in the generation of STOP in the library function.

Solution: add a command line of judging if the GENSTOP bit is cleared or not after configuring STOP, and then execute next operation.

```

/* generate stop condition */
i2c_stop_generate(hi2c->i2cx);
/* wait for the stop flag to be reset */
hi2c->status = i2c_wait_flag(hi2c, I2C_STOPF_FLAG, RESET, I2C_EVENT_CHECK_NONE,
hi2c->timeout);
    
```

Type: MCU application

Applicable products: AT32 series

Main function: I2C

Minor function: None

Document revision history

Date	Revision	Changes
2022.2.16	2.0.0	Initial release

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