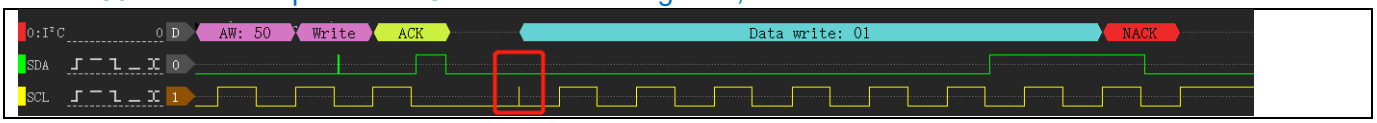
FAQ0033
Frequently Asked Questions

80ns pulse present on SCL while I2C writes data

Questions:

When AT32's I2C is in master mode and other MCUs in slave mode, after address is sent, there will have around 80ns abnormal pulse on SCL line when writing data, as shown below:

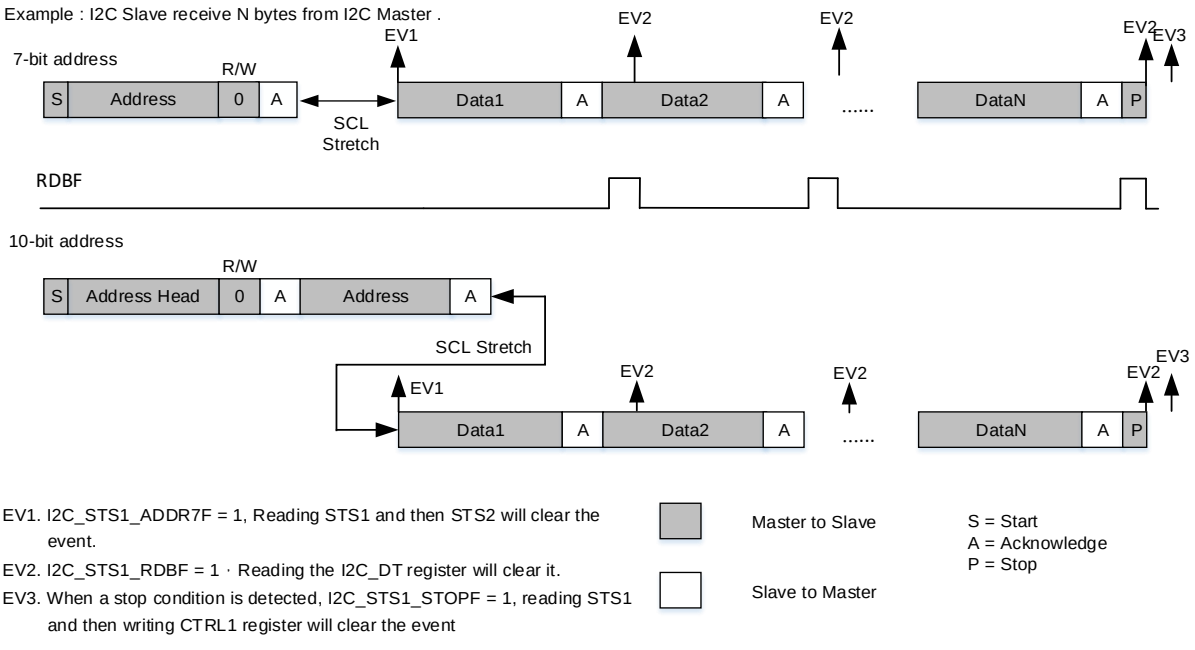


Answer:

The reason for this is that in master/slave mode, the slave is unable to release SCL line during the period of master being in high level.

How to resolve this problem?

Example: use an interrupt event to operate AT32 I2C, the timing diagram during ADDR stage is as follows:



It can be seen from the figure above that slave enters interrupt after detecting a correct ADDR on EV1 event, and releases SCL line only after ADDRF flag bit is cleared by reading status registers STS1 and STS2. If this is the case, this operation may cause unwanted problems. As a result, one of the more reliable ways is to let slave releases SCL line before the SCL is controlled by master. This can be done by modifying master code or slave code.

1. Modifying master code: first evaluate the duration time the slave takes from entering an I2C interrupt and processing it and then clearing ADDRF flag, then add a period of delay (depending on slave) before sending data:

```
/* wait for the addr7 flag to be set */
if(i2c_wait_flag(hi2c, I2C_ADDR7F_FLAG, RESET, I2C_EVENT_CHECK_NONE, timeout) != I2C_OK)
{
    /* disable ack */
    i2c_ack_enable(hi2c->i2cx, FALSE);
    return I2C_ERR_STEP_2;
}

delay_us(1);
/* clear addr flag */
i2c_addr_flag_clear(hi2c);
```

2. Modifying slave mode: after ADDR is sent by master, the slave's ACK is controlled by hardware. At this point, if the slave is unable to enter I2C interrupt because of being busy with processing other interrupt functions, then SCL line would be hold. This is why it is necessary to give the highest priority to I2C in order to respond to I2C interrupt quickly. For example, divide NVIC 4 bit into 2:2, the I2C event interrupt should be given with the highest priority.

```
/* config nvic priority group */
nvic_priority_group_config(NVIC_PRIORITY_GROUP_2);

/* configure and enable i2c interrupt */
nvic_irq_enable(I2Cx_EVT_IRQn, 0, 0);
```

Additionally, it is necessary to minimize the number of codes from entering I2C interrupt to clearing ADDRF flag to shorten the SCL hold time, so that the ADDRF is cleared as soon as it is detected.

```
if(i2c_wait_flag(hi2c, I2C_ADDR7F_FLAG, RESET, I2C_EVENT_CHECK_NONE, timeout) != I2C_OK)
{
    /* disable ack */
    i2c_ack_enable(hi2c->i2cx, FALSE);
    return I2C_ERR_STEP_2;
}

/* clear addr flag */
i2c_addr_flag_clear(hi2c);
```

In fact, all I2C events which could hold SCL line (such as, the bus receives data but has no sufficient time to read from DT register) should be handled as quickly as possible to reduce SCL hold time.

Type: MCU applications
Applicable products: AT32F403A
Main function: I2C
Minor function: None

Document revision history

Date	Revision	Changes
2022.2.16	2.0.0	Initial release

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