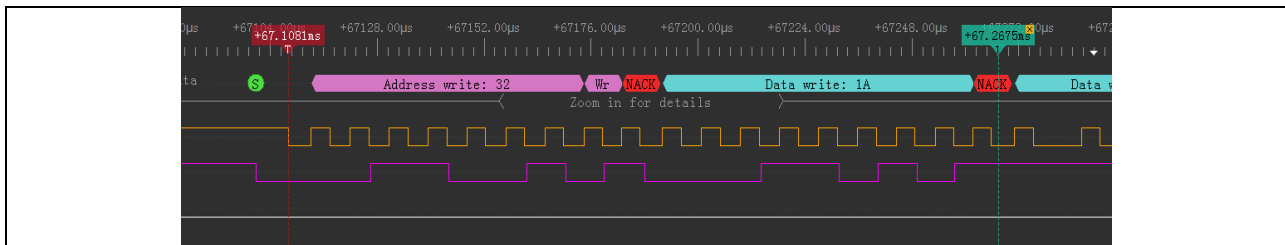# Wrong SPEED bit configuration triggers communication failure
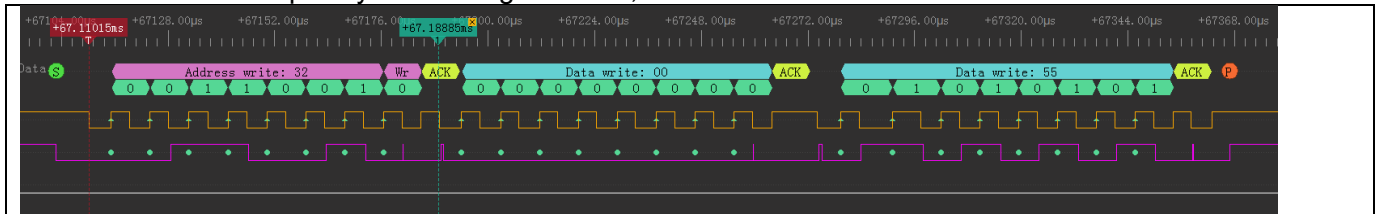
Questions:

In I2C slave mode, if the SPEED bit of the I2C_CLKCTRL register is written with an incorrect value, this would cause communication error.

Answer：

In slave mode, a wrong configuration to the SPEED bit of the I2C_CLKCTRL register causes communication failure without ACK response, as shown below:

In slave mode, this bit (SPEED default value is 0) should not be configured or calculated based on actural APB clock and I2C frequency. After fixing the code, communication work resumes.

Type: MCU applications

Applicable products: AT32F403, AT32F415, AT32F413, AT32F403A, AT32F407, AT32F421

Main function: I2C

Minor function: None

Document revision history

Date	Revision	Changes
2022.2.16	2.0.0	Initial release

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