

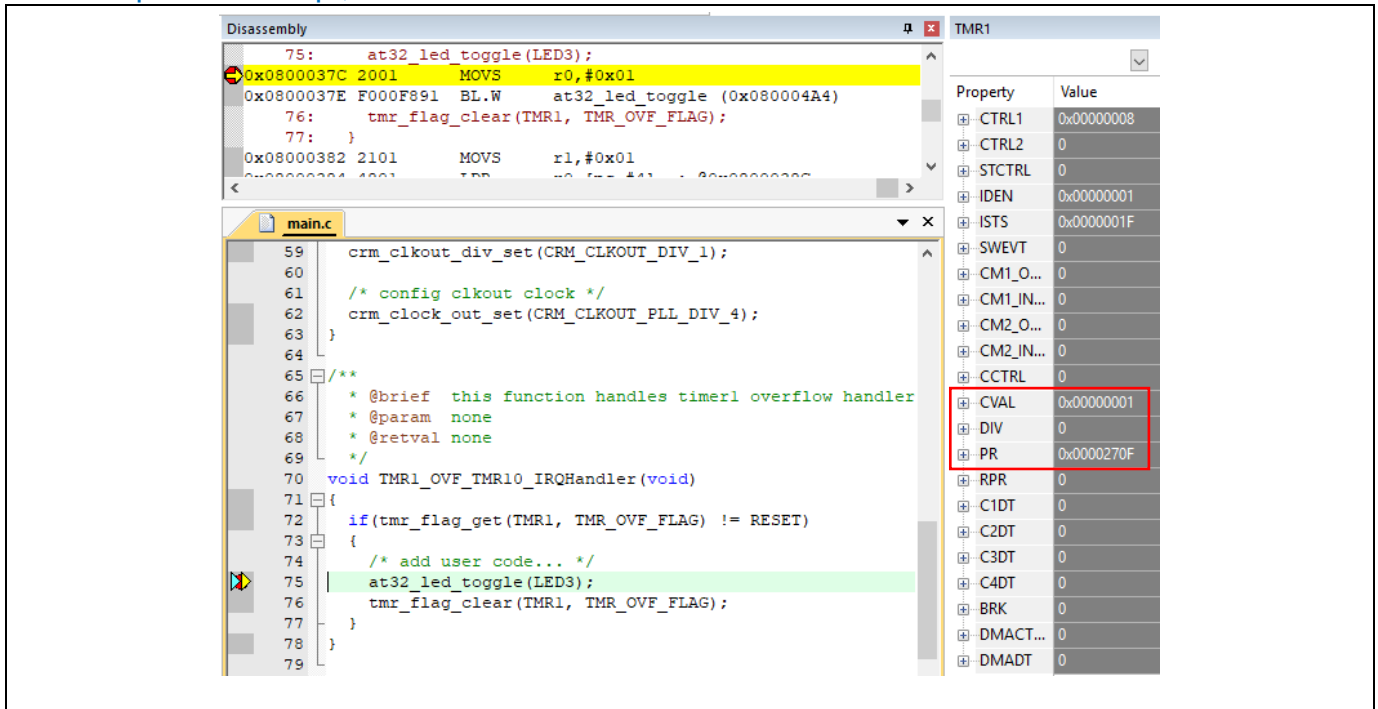
FAQ0046

Frequently Asked Questions

TMR_CVAL starts counting from 1 in one-pulse mode

Questions:

In one-pulse mode, when the TMRx_PR register is set as an odd number and TMRx_DIV as 0, overflow update interrupt is generated. Then the TMRx_CVAL starts counting from 1 after the second update interrupt, as shown below:



Answer:

1. Set the TMRx_PR register as an even number
2. Set the TMRx_DIV as a non-zero value

Either option is fine.

Type: MCU applications

Applicable products: AT32F403, AT32F413

Main function: TMR

Minor function: None

Document revision history

Date	Revision	Changes
2022.2.16	2.0.0	Initial release

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