FAQ0055
Frequently Asked Questions

How to understand the calculation formula of CAN baud rate?

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Baud rate calculation formula

$$BaudRate = \frac{1}{\text{Nomal Bit Timimg}}$$

$$Nomal\ Bit\ Timing = t_{SYNC\_SEG} + t_{BSEG1} + t_{BSEG2}$$

with

$$t_{SYNC\_SEG} = 1\ x\ t_q$$

$$t_{BSEG1} = (1 + \text{BTS1}[3{:}\ 0])\ x\ t_q$$

$$t_{BSEG2} = (1 + \text{BTS2}[2{:}\ 0])\ x\ t_q$$

$$t_q = (1 + \text{BRDIV}[11{:}\ 0])\ x\ t_{pclk}$$

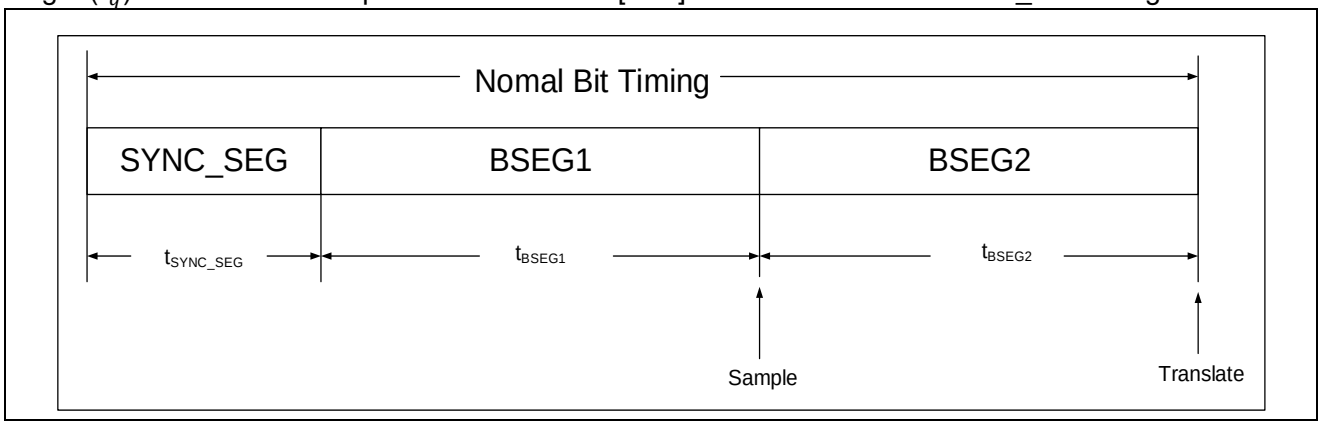
Where, , t_q refers to a time unit, t_{PCLK} = APB clock cycle

Answer:

The nominal bit time of the CAN bus consists of three parts as follows:

1. Synchronization segment (SYNC_SEG): This segment has one time unit, that is the $1\ x\ t_q$.
2. Bit segment 1 (BIT SEGMENT 1): It is BSEG1 including the PROP_SEG and PHASE_SEG1 of the CAN standard. Its duration is between 1 and 16 time units, defined by the BTS1[3: 0] bit, that is, the $t_{BSEG1} = (1 + \text{BTS1}[3{:}\ 0])\ x\ t_q$
3. Big segment 2 (BIT SEGMENT 2): It is referred to as BSEG2 including the PHASE_SEG2 of the CAN standard. Its duration is between 1 and 8 time units, defined by the BTS2[2: 0] bit, that is, the $t_{BSEG2} = (1 + \text{BTS2}[2{:}\ 0])\ x\ t_q$

The length (t_q) of the time unit depends on the BRDIV[11:0] and PCLK bits in the CAN_BTMG register.



Deduced as follows based on the formula:

$$BaudRate = \frac{1}{1\ x\ t_q + t_{BSEG1} + t_{BSEG2}}$$

$$= \frac{1}{t_q + (1 + BTS1[3:0])\ x\ t_q + (1 + BTS2[2:0])\ x\ t_q}$$

$$= \frac{1}{t_q\ x\ (1 + 1 + BTS1[3:0] + 1 + BTS2[2:0])}$$

$$= \frac{1}{(1 + BRDIV[11:0])\ x\ t_{pclk}\ x\ (3 + BTS1[3:0] + BTS2[2:0])}$$

$$= \frac{f_{pclk}}{(1 + BRDIV[11:0])\ x\ (3 + BTS1[3:0] + BTS2[2:0])}$$

Where, BRDIV[11:0], BTS1[3: 0] and BTS2[2:0] are the parameters of the CAN_BTMG register. Their respective BSP structure in AT32 BSP program are as follows:

CAN_BTMG registe	Functional descritpion	BSP structure
BRDIV[11:0]	baud rate divider	can_baudrate_struct.baudrate_div
BTS1[3:0]	occupy 1 time unit	can_baudrate_struct.bts1_size
BTS2[2:0]	occupy two time units	can_baudrate_struct.bts2_size

Example:

Assuming f_{SYSCLK}=192MHz, $f_{APB1CLK} = f_{PCLK}$=24MHz, the software configuration for 1M baud rate is as follows:

```
/* can baudrate, set baudrate = pclk/(baudrate_div *(1 + bts1_size + bts2_size)) */
can_baudrate_struct.baudrate_div = 2; /* BRDIV[11：0]=0x01 */
can_baudrate_struct.bts1_size = CAN_BTS1_8TQ; /* BTS1[3：0]=0x07,8 time quantum */
can_baudrate_struct.bts2_size = CAN_BTS2_3TQ; /* BTS2[2：0]=0x02,3 time quantum */
can_baudrate_set(CAN1, &can_baudrate_struct);
/* baudrate = 24M/( ( 1+0x01 ) * (1 + ( 1+0x07 ) + ( 1+0x02 ) ) ) = 1MHz */
```

Note: For convenience, the structure value in BSP has actually been increased by 1, and thus it has to be deducted by 1 when the structure is substituted into the register for calculation.

Type: MCU

Applicable products: AT32F403, AT32F403A, AT32F407, AT32F413, AT32F415

Main function: CAN

Minor function: None

Document revision history

Date	Revision	Changes
2022.3.10	2.0.0	Initial release

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