

Precautions on the use of Dual CAN filter

Questions:

What should we know about the use of Dual CAN filter?

Answer:

CAN1 and CAN2 are independent of each other. Both of them have their own 14 filter banks, which cannot be mixed. For example, when only CAN1 is used, the filter banks of CAN2 cannot be assigned to CAN1.

***21.7.3.6 CAN filter bank i filter bit register (CAN_ FiFBx) (i=0..13; x=1..2)**

Note: There are 14 filter banks (i=0..13). Each filter bank consists of two 32-bit registers, CAN_ FiFB[2:1]. This register can be modified only when the FAENx bit of the CAN_ FACFG register is cleared or the FCS bit of the CAN_ FCTRL register is set.

Bit	Register	Reset value	Type	Description
Bit 31: 0	FFDB	0xXXXX XXXX+rw		Filters filter data bit Identifier list mode: The configuration value of the register matches with the level of the corresponding bit of the data received on the bus (If it is a standard frame, the value of the corresponding bit of the extended frame is neglected.) Identifier mark mode: Only the bit with its register configuration value 1 can match with the level of the corresponding bit of the data received on the bus. It don't care when the register value is 0.

CAN	Register name	Base address offset	Reset value
CAN1	FB0F1	240h	0xFFFFFFFF
CAN2	FB0F2	244h	0xFFFFFFFF
CAN1	FB1F1	248h	0xFFFFFFFF
CAN2	FB1F2	24Ch	0xFFFFFFFF
...
CAN1	FB13F1	2A8h	0xFFFFFFFF
CAN2	FB13F2	2ACh	0xFFFFFFFF

Type: MCU

Applicable products: AT32F403, AT32F403A, AT32F413, AT32F407

Main function: CAN

Minor function: None

Document revision history

Date	Revision	Changes
2022.3.10	2.0.0	Initial release

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