

**FAQ0057**

## Frequently Asked Questions

## Precautions on AT32F403 enabling SDIO data transfer

**Questions:**

What are the requirements for AT32F403 enabling SDIO data transfer?

**Answer:**

The DCSM (data channel status machine) of SDIO\_DTCTRL register does not clear FIFO. In other words, when there are data pending for read or transmit in FIFO — there are still valid data in FIFO, enabling DCSM will cause the remaining data in FIFO to be sent immediately by hardware.

To avoid this happen, follow the procedures below:

1. Enable DCSM after the completion of reception or transmission operation
2. After disabling DCSM, clear FIFO through CMD12(STOP\_TRANSMISSION)

```
/******No card insertion, no response*****/  
SDIO1->cmdctrl=0x44C;  
while((SDIO1->sts&1<<2)!=1<<2);  
/******Card insertion, with response*****/  
SDIO1->cmdctrl=0x44C;  
while((SDIO1->sts&1<<6)!=1<<6);
```

**Type:** MCU applications

**Applicable products:** AT32F403

**Main function:** TMR

**Minor function:** None

**Document revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
2022.3.10	2.0.0	Initial release

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