

FAQ0071

Frequently Asked Questions

AT32F403 IO function priority level

Questions:

Each of IOs in AT32F403 has multiple function output, so is there any priority among them? Do we need to confirm which function output is given with high priority when in use?

Answer:

I/O function has priority level. Hardware enjoys the highest priority, followed by alternate functions. The basic principle is that analog signals take priority over digital signals, whereas output digital over input digital.

Example: if the 18th pin PF6 is used, it acts as ADC3_IN4/XMC_NIORD/TMR15_CH4, by default (see datasheet), and it can be remapped on TMR10_CH1.

Based on the table below, for PF6 pin, the highest priority is given to XMC_NIORD, followed by TMR10_CH1 and TMR15_CH4. In other words, if PF6 pin is using TMR15_CH4 while the program is using TMR10_CH1, then the TMR10_CH1 wins over TMR15_CH4. Similarly, if the XMC_NIORD is used, it will beat TMR10_CH1 and TMR15_CH4 in terms of priority.

Note that ADC3_IN4 is not included in the priority list as it is used as an input.

Table below lists the priority level of AT32403 I/O output.

LQFP144	Pin name	Hardware priority	AF priority (high->low)					
1	PE2	TRACECK	XMC_A23	SPI4_SCK				
2	PE3	TRACED0	XMC_A19					
3	PE4	TRACED1	XMC_A20	SPI4_CS				
4	PE5	TRACED2	XMC_A21	TMR9_CH1	SPI4_MISO			
5	PE6	TRACED3	XMC_A22	TMR9_CH2	SPI4_MOSI			
6	VBAT							
7	PC13	TAMPER_RTC						
8	PC14	LEXT_IN						
9	PC15	LEXT_OUT						
10	PF0		XMC_A0	TMR15_CH1				
11	PF1		XMC_A1	TMR15_CH1C				
12	PF2		XMC_A2	TMR15_CH2				
13	PF3		XMC_A3	TMR15_CH2C				
14	PF4		XMC_A4	TMR15_CH3				
15	PF5		XMC_A5	TMR15_CH3C				
16	VSS_5							
17	VDD_5							
18	PF6		XMC_NIORD	TMR10_CH1	TMR15_CH4			
19	PF7		XMC_NREG	TMR11_CH1	TMR15_EXT			
20	PF8		XMC_NIOWR	TMR13_CH1	TMR15_BRK			
21	PF9		XMC_CD	TMR14_CH1				
22	PF10		XMC_INTR					
23	HEXT_IN							
24	HEXT_OUT							

LQFP144	Pin name	Hardware priority	AF priority (high->low)					
25	NRST							
26	PC0		SDIO2_D0					
27	PC1		SDIO2_D1					
28	PC2		SDIO2_D2					
29	PC3		SDIO2_D3					
30	VSSA							
31	VREF-							
32	VREF+							
33	VDDA							
34	PA0-WKUP	WKUP	TMR2_CH1	TMR5_CH1	USART2_CTS			
35	PA1		TMR2_CH2	TMR5_CH2	USART2_RTS			
36	PA2		TMR2_CH3	TMR5_CH3	TMR9_CH1	USART2_TX	SDIO2_CK	
37	PA3		TMR2_CH4	TMR5_CH4	TMR9_CH2	SDIO2_CMD		
38	VSS_4							
39	VDD_4							
40	PA4		USART2_CK	SPI1_CS	SDIO2_D0	SDIO2_D4		
41	PA5		SPI1_SCK	SDIO2_D1	SDIO2_D5			
42	PA6		TMR3_CH1	TMR13_CH1	SPI1_MISO	SDIO2_D2	SDIO2_D6	
43	PA7		TMR3_CH2	TMR8_CH1C	TMR14_CH1	SPI1_MOSI	TMR1_CH1C	SDIO2_D3/ SDIO2_D7
44	PC4		SDIO2_CK					
45	PC5		SDIO2_CMD					
46	PB0		TMR3_CH3	TMR8_CH2C	TMR1_CH2C	I2S1_MCK		
47	PB1		TMR3_CH4	TMR8_CH3C	TMR1_CH3C	SPIM_SCK		
48	PB2/BOOT1							
49	PF11		XMC_NIOS16					
50	PF12		XMC_A6					
51	VSS_6							
52	VDD_6							
53	PF13		XMC_A7	TMR15_CH4				
54	PF14		XMC_A8	TMR15_EXT				
55	PF15		XMC_A9	TMR15_BRK				
56	PG0		XMC_A10	SPI1_MISO				
57	PG1		XMC_A11	SPI1_MOSI				
58	PE7		XMC_D4	TMR1_EXT				
59	PE8		XMC_D5	TMR1_CH1C				
60	PE9		XMC_D6	TMR1_CH1				
61	VSS_7							
62	VDD_7							
63	PE10		XMC_D7	TMR1_CH2C				
64	PE11		XMC_D8	TMR1_CH2	SPI4_SCK			
65	PE12		XMC_D9	TMR1_CH3C	SPI4_CS			
66	PE13		XMC_D10	TMR1_CH3	SPI4_MISO			

LQFP144	Pin name	Hardware priority	AF priority (high->low)					
67	PE14		XMC_D11	TMR1_CH4	SPI4_MOSI			
68	PE15		XMC_D12	TMR1_BRK				
69	PB10		USART3_TX	I2C2_SCL	TMR2_CH3			
70	PB11		USART3_RX	I2C2_SDA	TMR2_CH4			
71	VSS_1							
72	VDD_1							
73	PB12		USART3_CK	I2C2_SMBA	SPI2_CS			
74	PB13		TMR1_CH1C	SPI2_SCK	USART3_CTS			
75	PB14		TMR1_CH2C	TMR12_CH1	USART3_RTS	SPI2_MISO		
76	PB15		TMR1_CH3C	TMR12_CH2	SPI2_MOSI			
77	PD8		XMC_D13	USART3_TX				
78	PD9		XMC_D14	USART3_RX				
79	PD10		XMC_D15	USART3_CK				
80	PD11		XMC_A16	USART3_CTS				
81	PD12		XMC_A17	TMR4_CH1	USART3_RTS			
82	PD13		XMC_A18	TMR4_CH2				
83	VSS_8							
84	VDD_8							
85	PD14		XMC_D0	TMR4_CH3				
86	PD15		XMC_D1	TMR4_CH4				
87	PG2		XMC_A12	TMR15_CH1				
88	PG3		XMC_A13	TMR15_CH1C				
89	PG4		XMC_A14	TMR15_CH2				
90	PG5		XMC_A15	TMR15_CH2C				
91	PG6		XMC_INT2	TMR15_CH3				
92	PG7		XMC_INT3	TMR15_CH3C				
93	PG8							
94	VSS_9							
95	VDD_9							
96	PC6		TMR8_CH1	I2S2_MCK	SDIO1_D6	TMR3_CH1		
97	PC7		TMR8_CH2	I2S3_MCK	SDIO1_D7	TMR3_CH2		
98	PC8		TMR8_CH3	SDIO1_D0	TMR3_CH3	I2S4_MCK		
99	PC9		TMR8_CH4	SDIO1_D1	TMR3_CH4	I2C3_SDA		
100	PA8		TMR1_CH1	CLKOUT	USART1_CK	I2C3_SCL	SPIM_CS	
101	PA9		TMR1_CH2	USART1_TX	I2C3_SMBA			
102	PA10		TMR1_CH3	USART1_RX				
103	PA11	USBFS1_D+	TMR1_CH4	SPIM_IO0	USART1_CTS			
104	PA12	USBFS1_D-	CAN1_TX	USART1_RTS	SPIM_IO1	TMR1_EXT		
105	PA13	JTMS-SWDIO						
106								
107	VSS_2							
108	VDD_2							

LQFP144	Pin name	Hardware priority	AF priority (high->low)					
109	PA14	JTCK-SWCLK						
110	PA15	JTDI	SPI3_CS	TMR2_CH1	SPI1_CS			
111	PC10		UART4_TX	SDIO1_D2	USART3_TX			
112	PC11		UART4_RX	SDIO1_D3	UART3_RX			
113	PC12		UART5_TX	SDIO1_CK	USART3_CK			
114	PD0	OSC_IN(64PIN 及以下)	XMC_D2					
115	PD1	OSC_OUT (64PIN 及以下)	CAN1_TX	XMC_D3				
116	PD2		SDIO1_CMD					
117	PD3		XMC_CLK	USART2_CTS				
118	PD4		XMC_NOE	USART2_RTS				
119	PD5		XMC_NWE	USART2_TX				
120	VSS_10							
121	VDD_10							
122	PD6		XMC_NWAIT	USART2_RX				
123	PD7		XMC_NCE2 / XMC_NE1	USART2_CK				
124	PG9		XMC_NCE3 / XMC_NE2					
125	PG10		XMC_NCE4_1 / XMC_NE3					
126	PG11		XMC_NCE4_2					
127	PG12		XMC_NE4					
128	PG13		XMC_A24					
129	PG14		XMC_A25					
130	VSS_11							
131	VDD_11							
132	PG15							
133	PB3	JTDO/TRACESWO	SPI3_SCK	TMR2_CH2	SPI1_SCK			
134	PB4	NJTRST	SPI3_MISO	TMR3_CH1	SPI1_MISO	I2C3_SDA		
135	PB5		I2C1_SMBA	SPI3_MOSI	TMR3_CH2	SPI1_MOSI		
136	PB6		TMR4_CH1	I2C1_SCL	USART1_TX	SPIM_I03		
137	PB7		TMR4_CH2	I2C1_SDA	XMC_NADV	SPIM_I02		
138	BOOT0							
139	PB8		TMR4_CH3	TMR10_CH1	SDIO1_D4	I2C1_SCL		
140	PB9		CAN1_TX	TMR4_CH4	TMR11_CH1	SDIO1_D5	I2C1_SDA	
141	PE0		XMC_LB					
142	PE1		XMC_UB					
143	VSS_3							
144	VDD_3							

Type: MCU applications

Applicable products: AT32F403

Main function: I/O functions

Minor function: None

Document revision history

Date	Revision	Changes
2022.2.17	2.0.0	Initial release

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