FAQ0072
Frequently Asked Questions

Alternate function pin release conditions

Questions:

For AT32F413/AT32F415/AT32F403A/AT32F407, under what conditions can these alternate function pins be released for TMR?

Answer:

For example:

When the USART1 is being used, if the user wants to use the alternate function TMR1_CH1 on the USART1_CK (PA8) pin, he needs to check the table below, where the “CK “ of USART is marked “YES”, meaning that TMR1_CH1 can be used as alternate function while USART1 is in use, on the condition of CLKEN=0.

Similarly, if the user wants to use the alternate function TMR1_CH2 on the USART1_TX (PA9) pin, he needs to check the table below, where the “TX” of USART is marked “NO”, meaning that the TMR1_CH2 cannot be used as alternate function while USART1 is working.

AT32F413xx/AT32F415xx/AT32F403Axx/AT32F407xx: Alternate function pin release rule			
	OUTPUT pin	**Can AT32 be released? (Judge: Whether the TIMER can be output after release)**	**Release conditions**
SPI	SCK	NO	NC
	MCK	**YES**	**Release when MCKOE=0**
	MOSI/I2S_SD	NO	NC
	MISO	NO	NC
	NSS	NO	NC
SDIO	CK	NO	NC
	CMD	NO	NC
	D0	NO	NC
	D1	NO	NC
	D2	NO	NC
	D3	**YES**	Release in one-bit bus mode
	D4	**YES**	Release when bus width is in non-8-bit bus mode
	D5	**YES**	Release when bus width is in non-8-bit bus mode
	D6	**YES**	Release when bus width is in non-8-bit bus mode
	D7	**YES**	Release when bus width is in non-8-bit bus mode
USART	TX	NO	NC
	CK	**YES**	**Release when CLKEN=0**
	RTS	**YES**	**Release when RTSE=0**
I2C	SCL	NO	NC
	SDA	NO	NC
	SMBA	**YES**	**Release when PERMODE=0 (I2C mode)**
SPIM	SPIM_SCK	NO	NC
	SPIM_CS	NO	NC
	SPIM_IO0	NO	NC
	SPIM_IO1	NO	NC

AT32F413xx/AT32F415xx/AT32F403Axx/AT32F407xx: Alternate function pin release rule			
OUTPUT pin		**Can it be released? (Judge: Whether the TIMER can be output after release)**	**Release conditions**
	SPIM_IO2	NO	NC
	SPIM_IO3	NO	NC
CAN	TX	NO	NC
XMC	XMC_NE[4:1]	YES	The bit 0 in the four registers 0xA0000000+8* (x-1), x=1…4 selects the corresponding NE signal. Those unselected can be released.
	XMC_NADV	NO	NC
	XMC_LB/ XMC_UB	YES	It is occupied as long as bank1 is used.
	XMC_CLK	YES	This pin is occupied when any one of the bit 0 in the register 0xA0000000+8* (x-1) ,x=1…4, is enabled and bit 19 or bit 8 of the ctrl register is enabled. Otherwise, it is released.
	XMC_A[25:0]	YES (AT32F403A is slightly different from the rule. XMC_A[25:0] output has the same priority as the TMR output, so both would output simultaneously, that is, TIMER will interfere with XMC_A[25:0] output; This situation needs to be avoided during actual application because two blocks are used at the same time.)	For 0xA0000000+0x40+0x20* (x-1), x=2…4 register, only A16 and A17 are occupied when the bit 2 is enabled and the bit 3 is set to select nand Flash. For 0xA0000000+0x40+0x20* (x-1) ,x=2..4 register, only A[10:0] is occupied when the bit 2 is enabled and bit 3 is cleared to select PC card. For 0xA0000000+8* (x-1) ,x=1…4, this pin is occupied as long as bank1 is used.
	XMC_D[7:0]	NO	
	XMC_NOE	NO	
	XMC_NWE	NO	
	XMC_NWAIT	NO	
	XMC_NCE[3:2]	YES	For 0xA0000000+0x40+0x20* (x-1), x=2…4 , when bit2 is enabled, x=2 corresponds to NCE2 pin, x=3 corresponds to NCE3 pin.
	XMC_NCE4_1	YES	This pin is occupied when the bit 2 in the 0xA0000000+0x40+0x20* (x-1), x=2…4, is enabled and x=4.
	XMC_NCE4_2	YES	This pin is occupied when the bit 2 in the 0xA0000000+0x40+0x20* (x-1), x=2…4, is enabled and x=4.
	XMC_D[15:8]	YES (AT32F403A is slightly different from the rule. The IO is not always occupied by XMC_D[15:8] so that the TIMER output would occur at the same time while XMC_D[15:8] is used, that is, TIMER will interfere with XMC_D[15:8] output. This situation needs to be avoided during actual application because two blocks are used at the same time.)	For 0xA0000000+0x40+0x20* (x-1) , x=2…4 , when bit2 is enabled , x=2,3, and bit3=1, bit[5:4]=0, D[15 : :8] can be released.
ETH MAC	ETH_MDC	NO	NC
	ETH_MII_TXD2	YES	Release in RMII mode
	ETH_MDIO	NO	NC
	ETH_MII_TX_EN/ ETH_RMII_TX_EN	NO	NC
	ETH_MII_TXD0/ ETH_RMII_TXD0	NO	NC
	ETH_MII_TXD1/ ETH_RMII_TXD1	NO	NC
	ETH_PPS_OUT	**YES**	Release when AFIO_MAP 的 PTP_PPS_REMAP=0.
	ETH_MII_TXD3	YES	Release in RMII mode

Type: MCU
Applicable products: AT32F413, AT32F415, AT32F403A, AT32F407
Main function: I/O alternate function
Minor function: None

Document revision history

Date	Revision	Changes
2022.2.17	2.0.0	Initial release

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