**FAQ0124**

Frequently Asked Questions

# How to use AT32F43x_ADC shift mode

## Questions:

For AT32F43x, in ADC regular shift mode, its conversion time at certain configuration conditions is one ADCCLK clock longer than its theoretical value.

## Example:

In 12-bit precision and in repeation mode of single-salve regular shift mode

When the application sets the sampling time of a channel to ADC_SAMPLETIME_2_5, it means that the shift length is 5.

In theory, the sampling/conversion interval between two adjacent channels of the same ADC should be 15 ADCCLK, but the actual test result turns out to be 16 ADCCLK.

## Answer:

Such scenario is designed by ARTERY to guarantee data integrity.

In other words, “In ADC regular shift mode, when the sample time of one ADC overlaps with another ADC’ conversion time, starting a new sampling may lead to inaccurate voltage and cause converted data to fluctuate within a small range (usually 1 LSB). Our design is to let the ADC under conversion stop for 1 ADCCLK before restarting conversion so as to eliminate this fluctuation and ensure data integrity”

Of which, “this additional 1 ADCCLK can be done through software”, see below:

```
/*Execute code during ADC initialization*/
*(volatile uint32_t *)0x400123AC |= (0x1 << 0);
```

**Type:** MCU application
**Applicable products:** AT32F435, AT32F437
**Main function:** ADC
**Other function:** None

**Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 2022.3.4 | 2.0.0 | Initial release |