MG0003
Migration Guide

Migrating from SXX32F103 to AT32F413

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing SXX32F103 series to AT32F413 series device. It puts together the most important information and lists the vital aspects that need to be taken into account.

To move an application from SXX32F103 series to AT32F413 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F413xx

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1 Similarities and differences between AT32F413 and SXX32F103

The AT32F413 series microcontrollers are basically compatible with the SXX32F103 series and provide many enhanced features, except for some minor differences from the SXX32F103 series. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: The same package has the same pin definition. For extended peripherals, the alternate function of pins are defined.
- Addressing space: Memory and registers have the same logical addresses. Extended peripherals occupy the reserved space of SXX32 series.
- Compiler tools: identical, for example, Keil, IAR

1.2 Overview of differences

Table 1. Differences between SXX32F103 and AT32F413

	AT32F413	SXX32F103xC/xB/x8
Core	Cortex-M4, DSP instruction and Floating Point Unit (FPU)	Cortex-M3
System clock	Max frequency 200 MHz, APB1 100 MHz, APB2 100 MHz	Max frequency 72 MHz, APB1 36 MHz, APB2 72 MHz
Startup	8 ms	2.5 ms
Reset	3.6 ms	-
Wake up from Standby mode	3.6 ms	50 us
SRAM size	Extendable up to 64 KB	SXX32F103xC (48KB) SXX32F103xB (20KB) SXX32F103x8 (20KB)
External SPI Flash	Support up to 16 MB external SPI Flash (SPIM)	Not support
Boot Memory	18 KB Boot memory, including features such as: 1. USB DFU ISP programming 2. SPIM ISP programming 3. CRC check for Flash memory contents	6KB/2KB by part number
User System Data	48 Byte User System Data, including features such as: 1. SRAM mode settings 2. 8 Byte SPIM encryption key 3. Custom field (such as developer ID)	16 Byte
Flash memory 16-bit write time	50 µs	52.5 µs
Flash memory sector erase time	50 ms (AT32F413xC) 40 ms (AT32F413xB/x8)	40 ms

	AT32F413	SXX32F103xC/xB/x8
Flash memory mass erase time	800 ms	40 ms
sLib settings	Support	NA
Battery powered register	42 x half-byte data registers	10 x for small and medium density
SPI1 can be used as I2S	SPI1 can also be used as I2S	SPI1 can only be used as SPI
I2S support	48 pin has I2S feature	48 pin has no I2S feature
32-bit timer	TMR2 and TMR5 are 32-bit timers	All 16 bit
USB buffer	Extendable up to 1280 Byte	512 Byte
ADC	2 Msps (max ADCCLK=28MHz)	1 Msps (max ADCCLK=14MHz)
Temperature sensor	Positive temperature factor	Negative temperature factor
Voltage range	2.6V~3.6V	2.0V~3.6V
Core voltage	1.2V (lower current)	1.8V
ESD parameters	HBM:5KV, CDM:1000V	HBM:2KV, CDM:500V
Run mode	28.4 mA @ 72 MHz	51 mA @ 72 MHz
Power consumption at Sleep mode	23.9 mA @ 72 MHz	29.5mA @ 72 MHz
Power consumption at Deepsleep mode	490 uA	25 uA
Power consumption at Standby mode	9.9 uA	2.1 uA

2 Hardware migration

The migration from SXX32F103 to AT32F413 series is very simple as they are pin-to-pin compatible basically.

3 Software migration

3.1 Functional enhancement

This section describes the enhanced peripheral features of AT32F413 versus SXX32F103. The subsection presents the behavior of the AT32F413.

3.1.1 High frequency PLL settings

- AT32F413 embeds a PLL that can output up to 200 MHz clock
- PLL supports two frequency bands, bordered by 72 MHz. Its frequency can be up to 200 MHz by setting the PLLRANG register according to the output frequency
- When the embedded PLL is greater than 108 MHz in AT32F413, it is necessary to use auto step-by-step frequency switching feature.

3.1.2 PLL prescaler

- USB prescaler supports /2, /2.5, /3, /3.5, /4 output
- ADC prescaler supports /12, /16 output
- Clock output (CLKOUT) supports LICK, LEXT, PLLCLK/4, USB48M, ADCCLK, and the frequency-divided output.

3.1.3 ARM® 32-bit Cortex®-M4F with FPU

- Memory Protection Unit (MPU)
- Built-in single-cycle multiplication and hardware division
- Built-in Floating Point Unit (FPU)
- DSP instruction set

3.1.4 Security library

- Security library (sLib) feature is provided to prevent important IP-code from being modified or read by end applications so as to enhance security level.

3.1.5 Internal memory size extension

- Internal memory can be extended from 16 KB or 32 KB to 64 KB, causing the address range of the corresponding zero-wait Flash memory to change.

3.1.6 External SPI Flash (SPIM feature)

- Support external Flash (address range 0x0840_0000~0x093F_FFFF) via SPIM Flash interface

3.1.7 32-bit timers

- TMR2/TMR5 can be configured as 32-bit timers.

3.1.8 SPI1 used as I2S1

- SPI1 can be used as I2S1 as an alternate function

3.1.9 USBDEV buffer

- USB device (USBDEV) buffer can be extended up to 1280 Byte.

3.1.10 DMA channel flexible mapping

- DMA1 and DMA2 both enjoy flexible channel mapping features. In other words, the DMA request of a peripheral can be mapped onto any one DMA channel, making it flexible to allocate DMA channels.

3.1.11 CRC peripheral

- AT32 CRC peripheral allows to reverse the bit position of input data according to a given data format (byte, half-word or word). In other words, the upper bit of an input data is reversed to a lower bit, and so on.
- AT32 CRC peripheral supports reversing the bit location of an output data according to the full-word format. In other words, the upper bit of an output data is reversed to a lower bit, and so on.

3.2 Functional differences

This section describes the functional differences in terms of peripherals between AT32F413 and SXX32F103. The behavior of the AT32F413 is detailed in subsections.

3.2.1 Internal temperature sensor

- Temperature sensor has positive temperature factors.

3.2.2 GPIO 5V-tolerant pin compatibility

- PA11 and PA12 on all packages, and PD0 and PD1 on 64-pin/48-pin packages are not 5V tolerant, so the input level of these pins must not exceed VDD + 0.3V.

3.2.3 GPIO 5V-tolerant pin characteristics

- In floating input mode, 5V-tolerant pins still have around 10 μA of pull-up capability so that they may remain about 2.0V voltage, which is regarded as high level by the pin input logic.

3.2.4 Non 5V-tolerant GPIO pin limitations

- For non 5V-tolerant GPIO pins, injecting a voltage higher than VDD + 0.3V will result in GPIO exception.

3.2.5 PA11/PA12 weak pull-down resistor auto enable in Standby mode

- Each of PA11 and PA12 has a weak pull-down resistor of 330 kΩ that is automatically enabled by hardware in Standby mode.

3.2.6 BOOT0 with a pull-down resistor

- BOOT0 embeds a pull-down resistor of around 90 KΩ (cannot be disabled), therefore it is not necessary to add an external pull-down resistor while using BOOT0 pin.

3.2.7 PA0 pull-down resistor auto enable in Standby mode

- When the Standby mode is being entered, the pull-down resistor of PA0 pin is automatically enabled by internal control circuitry of the chip. The reason of this is to avoid current leakage caused by pin floating.

3.2.8 PVM interrupt generation if PVMEN bit is ON

- In case of VDD/VDDA=3.3V, an interrupt is generated when VDD is greater than PVM threshold each time the PVMEN bit changes from OFF to ON.

3.2.9 USB_DP with internal pull-up resistor

- USB_DP has an internal pull-down resistor supporting full-speed device. With this, users do not need an external 1.5kΩ pull-up resistor.

3.2.10 Dual CAN filter banks

- CAN1 and CAN2 are mutually independent, each of which has a fixed set of 14 filter banks.

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
2022.02.25	2.0.0	Initial release
2022.10.19	2.0.1	Added *3.1.10 DMA channel flexible mapping* Added *3.1.11 CRC peripheral*

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