MG0005
Migration Guide

Migrating from SXX32F0xx&GX32F3x0 to AT32F415

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing SXX32F0xx/GX32F3x0 series to AT32F415 series device. It puts together the most important information and lists the vital aspects that need to be taken into account.

To move an application from SXX32F0xx/GX32F3x0 series to AT32F415 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F415xx

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1 Similarities and differences between AT32F415 and SXX32F0xx/GX32F3x0

AT32F415 series microcontrollers are mostly compatible with the SXX32F0xx and GX32F3x0 series. In consideration of the overall cost-effectiveness, some functional trade-offs are made and many features are enhanced, causing some differences between them, which are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are basically the same for the same packages. For extended peripherals, define the alternate function of the pins
- Compiler tools: identical, for example, Keil, IAR

1.2 Overview of differences

Table 1. Summary of differences

	AT32F415	SXX32F0xx	GX32F3x0
Core	Cortex-M4	Cortex-M0	Cortex-M4
System clock	Max frequency 150 MHz, APB1 75 MHz, APB2 75 MHz	Max frequency 48MHz, APB 48MHz	Max frequency 108 MHz, APB1 54 MHz, APB2 54 MHz
Wake up from Deepsleep mode (voltage regulator is in low-power mode)	360 us	Max 9 us	-
Wake up from Standby mode	600 us	60.4 us	37.9 ms
SRAM size	32 KB	16 KB	4/6/8/16 KB by part number
Boot Memory	18KB boot memory, including such features as: 1. USB DFU ISP programming 2. CRC check of the contents of Flash memory	12KB	3KB
Flash memory 16-bit write time	42 us	60 us	86 us
Flash memory page erase time	8 ms	40 ms	300 ms
Flash memory mass erase time	10 ms	40 ms	1.6 s
Security library settings	Support	NA	NA
Battery powered register	20 x 32-bit battery powered registers	5 x 32-bit backup registers	5 x 32-bit backup registers
32-bit general-	TMR2 and TMR5 are 32-bit	TMR2 only	TMR2 only

	AT32F415	SXX32F0xx	GX32F3x0
purpose timer	timers		
16-bit general-purpose timer	TMR3, 4, 9, 10, 11	TMR3, 14, 15, 16, 17	TMR3, 14, 15, 16, 17
Basic timer	NA	TMR6, 7	TMR6
HICK fine tune	Through ACC, only has USB input	Through CRS, optional external pins are TSC_SYNC, LSE and USB	Through CTC, optional external pins are CTC_SYNC, LXTAL and USB
WKUP pin	1	6	5
TAMPER_RTC pin	1	2	2
USB	USB OTG, without NOE pin	USB Device, with NOE pin	USB Device
4-wire SPI master	NA	NA	Support
Infrared transmitter	NA	Support	Support
Touch control	NA	Support	Support
ADC	2 Msps (max ADCCLK = 28 MHz)	1 Msps (max ADCCLK = 14MHz)	2.86 Msps (max ADCCLK = 40 MHz)
Voltage range	2.6 V~3.6 V	2.4 V~3.6 V	2.6 V~3.6V
Core voltage	1.2 V (lower operating current)	1.8 V	1.2 V
ESD parameters	HBM:5KV, CDM:1000V	HBM:2KV, CDM:500V	HBM:6KV, CDM:2000V
Run mode	16.9mA@48MHz	24.1mA@48MHz	11.99mA@48MHz
Power consumption at Sleep mode	13.3mA@48MHz	15.0mA@48MHz	5.36mA@48MHz
Power consumption at Deepsleep mode	680 uA	5.1 uA	92.0 uA
Power consumption at Standby mode	3.6 uA	2.3 uA	6.9 uA

2 Hardware migration

The migration from AT32F415 to SXX32F0xx/GX32F3x0 series is simple as because they are pin-to-pin compatible basically, with only a few pins being affected.

Table 2. Pin compatibility between AT32F415 and SXX32F0xx/GX32F3x0

AT32F415				SXX32F0xx				GX32F3x0			
QFN32	QFP48	QFP64	Pin	QFN32	QFP48	QFP64	Pin	QFN32	QFP48	QFP64	Pin
5	5	5	PD0->OSCIN	-	5	5	PF0->OSCIN	5	5	5	PF0->OSCIN
6	6	6	PD1->OSCOUT	-	6	6	PF1->OSCOUT	6	6	6	PF1->OSCOUT
-	-	18	PF4	-	-	18	VSS	-	-	18	PF4
-	-	19	PF5	-	-	19	VDD	-	-	19	PF5
-	35	47	PF6	-	35	47	VSS	-	35	47	PF6
-	36	48	PF7	-	36	48	VDDIO2	-	36	48	PF7

Table 3. Alternate function compatibility between AT32F415 and SXX32F0xx/GX32F3x0

	AT32F415	SXX32F0xx	GX32F3x0
Pin number	Alternate function	Alternate function	Alternate function
PC2	-	SPI2_MISO, I2S2_MCK	-
PC3	-	SPI2_MOSI, I2S2_SD	-
PA0	-	-	I2C2_SCL
PA1	-	-	I2C2_SDA
PA4	-	-	SPI2_NSS
PA6	-	USAER3_CTS, I2S1_MCK	I2S1_MCK
PC4	-	USART3_TX	-
PC5	-	USART3_RX	-
PB0	USART3_RTS	USART3_CK	USART2_RX
PB1	USART3_CTS	USART3_RTS	SPI2_SCK
PB10	-	SPI2_SCK, I2S_CK	-
PB13	-	I2C2_SCL	-
PB14	-	I2C2_SDA, I2S2_MCK	-
PC6	I2S2_MCK	-	I2S1_MCK
PA8	-	-	USART2_TX
PA9	-	-	I2C1_SCL
PA10	-	-	I2C1_SDA
PA13		-	SPI2_MISO
PA14	-	USART2_TX	SPI2_MOSI, USART2_TX
PA15	-	USART2_RX	USART2_RX
PD2	-	USART3_RTS	-
PB4	-	I2S1_MCK	-
PB9	-	SPI2_NSS, I2S2_WS	I2S1_MCK

3 Software migration

3.1 Peripheral comparison

In terms of peripherals, there are some differences between AT32F415 and SXX32F0x/GX32F3x0, and some of them are new designs for AT32F415. Therefore, it is necessary to modify peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 4. Peripheral compatibility analysis

Peripheral	SXX32F0x/GX32F3x0	AT32F415	Compatibility	
			Pinout	Firmware driver
SPI	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Partial compatibility
DEBUG	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Partial compatibility
EXINT	Y	Y	Identical	Partial compatibility
CEC	Y	NA	NA	NA
DMA	Y	Y	NA	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
PWC	Y	Y	NA	Partial compatibility
SDIO	NA	Y	NA	NA
USART	Y	Y	Identical	Partial compatibility
I2C	Y	Y	Identical	Partial compatibility
DAC	Y	NA	NA	NA
ADC	Y	Y	Identical	Partial compatibility
RTC	Y	Y	Identical	Partial compatibility
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	New GPIO	incompatible
CAN	NA	Y	NA	NA
USB OTG	NA	Y	NA	NA
Touch sensing	Y	NA	NA	NA
CMP	Y	Y	Identical	Partial compatibility
SCFG	Y	NA	NA	NA
IOMUX	NA	Y	NA	NA

For the perspective of performance optimization, deep-level adjustment has been made on the architecture of AT32F415. The peripheral addresses and bus assignment of the AT32F415 show some differences compared to SXX32F0xx/GX32F3x0, as shown in *Table 5*.

Table 5. Peripheral comparison

Peripheral	SXX32F0xx/GX32F3x0		AT32F415	
	Bus	Base address	Bus	Base address
TSC	AHB1	0x40024000	NA	NA
CRC		0x40023000	AHB	0x40023000
FLASH		0x40022000		0x40022000

Peripheral	SXX32F0xx/GX32F3x0		AT32F415	
	Bus	Base address	Bus	Base address
CRM		0x40021000		0x40021000
DMA		0x40020000		0x40020000
GPIOF	AHB2	0x48001400	APB2	0x40011C00
GPIOE		0x48001000	NA	NA
GPIOD		0x48000C00	APB2	0x40011400
GPIOC		0x48000800		0x40011000
GPIOB		0x48000400		0x40010C00
GPIOA		0x48000000		0x40010800
ACC	NA	NA		0x40015800
DEBUG	APB	0x40015800	NA	NA
TMR17		0x40014800		
TMR16		0x40014400		
TMR15		0x40014000		
USART1		0x40013800	APB2	0x40013800
SPI1		0x40013000		0x40013000
TMR1		0x40012C00		0x40012C00
ADC		0x40012400		0x40012400
EXINT(SCFG)		0x40010400		0x40010400
SCFG+CMP		0x40010000	NA	NA
CEC		0x40007800	APB1	0x40007800
DAC		0x40007400		0x40007400
PWC		0x40007000		0x40007000
CRS		0x40006C00	NA	NA
I2C2		0x40005800	APB1	0x40005800
I2C1		0x40005400		0x40005400
USART2		0x40004400		0x40004400
SPI2		0x40003800		0x40003800
WDT		0x40003000		0x40003000
WWDT		0x40002C00		0x40002C00
RTC		0x40002800		0x40002800
TMR14		0x40002000	NA	NA
TMR6		0x40001000		
TMR3		0x40000400	APB1	0x40000400
TMR2		0x40000000		0x40000000
USBFS SRAM		0x40006000	NA	NA
USBFS		0x40005C00		
TMR7		0x40001400		
TMR4	NA	NA	APB1	0x40000800
CAN	APB	0x40006400		0x40006400
UART5		0x40005000		0x40005000
UART4		0x40004C00		0x40004C00
USART3		0x40004800		0x40004800
DMA2	AHB1	0x40020400	AHB	0x40020400

Peripheral	SXX32F0xx/GX32F3x0		AT32F415	
	Bus	Base address	Bus	Base address
USBOTG	NA	NA		0x50000000
TMR11			APB2	0x40015400
TMR10				0x40015000
TMR9				0x40014C00
TMR5				0x40000C00
IOMUX				0x40010000

3.2 Functional enhancement

This section describes the enhanced peripheral features of AT32F415 versus SXX32F0xx/GX32F3x0. The subsection presents the behavior of the AT32F415.

3.2.1 High frequency PLL settings

- AT32F415 embeds a PLL that can output up to 150 MHz clock

3.2.2 PLL prescaler

- USB prescaler supports /2, /2.5, /3, /3.5, /4 output
- ADC prescaler supports /12, /16 output

3.2.3 Security library (sLib)

- Security library (sLib) feature is provided to prevent important IP-code from being modified or read by end applications so as to enhance security level.

3.2.4 32-bit timers

- TMR2/TMR5 can be configured as 32-bit timers.

3.2.5 USB interface

- AT3F415 supports USBOTG, while SxxF0xx/GxxF3x0 supports USBDEV only. Compared to SxxF0xx/GxxF3x0, the USB interface of AT32F415 is a new peripheral with more powerful performance.

3.3 Functional differences

This section describes the functional differences in terms of peripherals between AT32F415 and SXX32F0xx/GX32F3x0. The behavior of the AT32F413 is detailed in subsections.

3.3.1 CRM interface

The differences related to CRM (Clock and reset management) in the AT32F415 series versus SXX32F0xx/GX32F3x0 are presented in *Table 6*.

Table 6.CRM differences

CRM	SXX32F0xx	GX32F3x0	AT32F415
HICK	8MHz RC	8MHz RC	48MHz RC divided by 6
HEXT	4-32MHz	4-32MHz	4-25MHz
LICK	40KHz RC	40KHz RC	40KHz RC

LEXT	32.768KHz	32.768KHz	32.768KHz
HICK 14	Dedicated to ADC	NA	NA
HICK 28	NA	Dedicated to ADC	NA
HICK 48	48MHz RC	48MHz RC	48MHz RC
RTC CLK	LSI, LSE, HSE/32	LSI, LSE, HSE/32	LICK, LEXT, HEXT/128
Max System clock frequency	48MHz	108MHz	150MHz
CLKOUT	HSI14, SYSCLK, HIS, HSE, PLL/2, PLL, LSE, LSI, HSI48	HSI28, LSI, LSE, HIS, HSE, PLL, PLL/2	ADCCLK, USB48, SYSCLK, LICK, LEXT, HICK, HEXT, PLL/2

3.3.2 DMA interface

The differences related to DMA in the AT32F415 series versus SXX32F0xx/GX32F3x0 are presented in *Table 7*.

Table 7.DMA differences

Peripheral	DMA request	SXX32F0xx	GX32F3x0	AT32F415
TMR17	TMR17_UP TMR17_CH1	DMA_Channel1/DMA_Channel2 DMA_Channel1/DMA_Channel2	DMA_Channel1/DMA_Channel2 DMA_Channel1/DMA_Channel2	NA
TMR16	TMR16_UP TMR16_CH1	DMA_Channel3/DMA_Channel4 DMA_Channel3/DMA_Channel4	DMA_Channel3/DMA_Channel4 DMA_Channel3/DMA_Channel4	NA
TMR15	TMR15_UP TMR15_CH1 TMR15_TRIG TMR15_COM	DMA_Channel5 DMA_Channel5 DMA_Channel5 DMA_Channel5	DMA_Channel5 DMA_Channel5 DMA_Channel5 DMA_Channel5	NA
USART1	USART1_Rx USART1_Tx	DMA_Channel3/DMA_Channel5 DMA_Channel2/DMA_Channel4	DMA_Channel3/DMA_Channel5 DMA_Channel2/DMA_Channel4	DMA1_Channel5 DMA1_Channel4
SPI1	SPI1_Rx SPI1_Tx	DMA_Channel2 DMA_Channel3	DMA_Channel2 DMA_Channel3	DMA1_Channel2 DMA1_Channel3
TMR1	TMR1_UP TMR1_CH1 TMR1_CH2 TMR1_CH3 TMR1_CH4 TMR1_TRIG TMR1_COM	DMA_Channel5 DMA_Channel2/DMA_Channel6 DMA_Channel3/DMA_Channel6 DMA_Channel5/DMA_Channel6 DMA_Channel4	DMA_Channel5 DMA_Channel2 DMA_Channel3 DMA_Channel5 DMA_Channel4 DMA_Channel4 DMA_Channel4	DMA1_Channel5 DMA1_Channel2 DMA1_Channel3 DMA1_Channel6 DMA1_Channel4 DMA1_Channel4 DMA1_Channel4

Peripheral	DMA request	SXX32F0xx	GX32F3x0	AT32F415
		DMA_Channel4 DMA_Channel4		
ADC	ADC	DMA_Channel1 DMA_Channel2	DMA_Channel1 DMA_Channel2	DMA1_Channel1
DAC	DAC_Channel1 DAC_Channel2	DMA_Channel3 DMA_Channel4	DMA_Channel3	NA
I2C2	I2C2_Rx I2C2_Tx	DMA_Channel5 DMA_Channel4	DMA_Channel5 DMA_Channel4	DMA1_Channel5 DMA1_Channel4
I2C1	I2C1_Rx I2C1_Tx	DMA_Channel3/ DMA_Channel7 DMA_Channel2/ DMA_Channel6	DMA_Channel3 DMA_Channel2	DMA1_Channel7 DMA1_Channel6
SDIO	SDIO	NA	NA	DMA2_Channel4
USART2	USART2_Rx USART2_Tx	DMA_Channel5 DMA_Channel4	DMA_Channel5 DMA_Channel4	DMA1_Channel6 DMA1_Channel7
SPI2	SPI2_Rx SPI2_Tx	DMA_Channel4 DMA_Channel5	DMA_Channel4 DMA_Channel5	DMA1_Channel4 DMA1_Channel5
TMR6	TIM6_UP	DMA_Channel3	DMA_Channel3	NA
TMR3	TMR3_UP TMR3_CH1 TMR3_TRIG TMR3_CH3 TMR3_CH4	DMA_Channel3 DMA_Channel4 DMA_Channel4 DMA_Channel2 DMA_Channel3	DMA_Channel3 DMA_Channel4 DMA_Channel4 DMA_Channel2 DMA_Channel3	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 DMA1_Channel2 DMA1_Channel3
TMR2	TMR2_UP TMR2_CH1 TMR2_CH2 TMR2_CH3 TMR2_CH4	DMA_Channel2 DMA_Channel5 DMA_Channel3/DMA_Channel7 DMA_Channel1 DMA_Channel4/DMA_Channel7	DMA_Channel2 DMA_Channel5 DMA_Channel3 DMA_Channel1 DMA_Channel4	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7
TMR4	TMR4_UP TMR4_CH1 TMR4_CH2 TMR4_CH3	NA	NA	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5
UART4	UART4_Rx UART4_Tx	DMA_Channel6 DMA_Channel7	NA	DMA2_Channel3 DMA2_Channel5
USART3	USART3_Rx USART3_Tx	DMA_Channel6/DMA_Channel3 DMA_Channel7/DMA_Channel2	NA	DMA1_Channel3 DMA1_Channel2
TMR5	TMR5_UP TMR5_CH1	NA	NA	DMA2_Channel2 DMA2_Channel5

Peripheral	DMA request	SXX32F0xx	GX32F3x0	AT32F415
	TMR5_CH2			DMA2_Channel4
	TMR5_CH3			DMA2_Channel2
	TMR5_CH4			DMA2_Channel1
	TMR5_TRIG			DMA2_Channel1

3.3.3 Interrupt vectors

Table 8 presents the interrupt vectors and interrupt vector number in AT32F415 series versus SXX32F0xx/GX32F3x0.

Table 8. Interrupt vector differences

Position	SXX32F0xx	GX32F3x0	AT32F415
0	WWDG	WWDG	WWDT
1	PVD	PVD	PVM
2	RTC	RTC	TAMPER
3	FLASH	FLASH	ERTC
4	RCC	RCC	FLASH
5	EXTI0_1	EXTI0_1	CRM
6	EXTI2_3	EXTI2_3	EXINT0
7	EXTI4_15	EXTI4_15	EXINT 1
8	TSC	TSC	EXINT 2
9	DMA_CH1	DMA_CH1	EXINT 3
10	DMA_CH2_CH3	DMA_CH2_CH3	EXINT 4
11	DMA_CH4_CH5	DMA_CH4_CH5	DMA_CH1
12	ADC_COMP	ADC_COMP	DMA_CH2
13	TIM1_BRK_UP_TRG_COM	TIM1_BRK_UP_TRG_COM	DMA_CH3
14	TIM1_CC	TIM1_CC	DMA_CH4
15	TIM2	TIM2	DMA_CH5
16	TIM3	TIM3	DMA_CH6
17	TIM6_DAC	TIM6_DAC	DMA_CH7
18	TIM7	TIM7	ADC1
19	TIM14	TIM14	CAN1_TX
20	TIM15	TIM15	CAN1_RX0
21	TIM16	TIM16	CAN1_RX1
22	TIM17	TIM17	CAN_SE
23	I2C1	I2C1_EV	EXINT5_9
24	I2C2	I2C2_EV	TMR1_BRK_TMR9
25	SPI1	SPI1	TMR1_OVF_TMR10
26	SPI2	SPI2	TMR1_TRG_HALL_TMR11
27	USART1	USART1	TMR1_CH
28	USART2	USART2	TMR2
29	USART3_4	NA	TMR3
30	CEC_CAN	CEC_CAN	TMR4
31	USBFS	Reserved	I2C1_EVT
32	Reserved	I2C1_ER	I2C1_ETR

Position	SXX32F0xx	GX32F3x0	AT32F415
33	Reserved	Reserved	I2C2_EVT
34	Reserved	I2C2_ER	I2C2_ERR
35	Reserved	Reserved	SPI1
36	Reserved	Reserved	SPI2
37	Reserved	Reserved	USART1
38	Reserved	Reserved	USART2
39	Reserved	Reserved	USART3
40	Reserved	Reserved	EXINT10_15
41	Reserved	Reserved	ERTCAlarm
42	Reserved	USBFS_Wakeup	Reserved
43	Reserved	Reserved	Reserved
44	Reserved	Reserved	Reserved
45	Reserved	Reserved	Reserved
46	Reserved	Reserved	Reserved
47	Reserved	Reserved	Reserved
48	Reserved	DMA_CH6_CH7	Reserved
49	Reserved	Reserved	SDIO
50	Reserved	Reserved	TMR5
51	Reserved	Reserved	Reserved
52	Reserved	Reserved	UART4
53	Reserved	Reserved	UART5
54	Reserved	Reserved	Reserved
55	Reserved	Reserved	Reserved
56	Reserved	Reserved	DMA2_CH1
57	Reserved	Reserved	DMA2_CH2
58	Reserved	Reserved	DMA2_CH3
59	Reserved	Reserved	DMA2_CH4_5
60	Reserved	Reserved	Reserved
61	Reserved	Reserved	Reserved
62	Reserved	Reserved	Reserved
63	Reserved	Reserved	Reserved
64	Reserved	Reserved	Reserved
65	Reserved	Reserved	Reserved
66	Reserved	Reserved	Reserved
67	Reserved	Reserved	USBOTG
68	Reserved	Reserved	Reserved
69	Reserved	Reserved	Reserved
70	Reserved	Reserved	COMP1
71	Reserved	Reserved	COMP2
72	Reserved	Reserved	ACC
73	Reserved	Reserved	Reserved
74	Reserved	Reserved	Reserved
75	Reserved	Reserved	Reserved
76	Reserved	Reserved	Reserved

Position	SXX32F0xx	GX32F3x0	AT32F415
77	Reserved	Reserved	Reserved
78	Reserved	Reserved	Reserved
79	Reserved	Reserved	Reserved
80	Reserved	Reserved	Reserved
81	Reserved	Reserved	Reserved
82	Reserved	Reserved	Reserved
83	Reserved	USBFS_Global	Reserved

3.3.4 EXINT interrupt source selection

For the configuration of external interrupts, there are some differences between AT32F415 series and SxxF0xx/GxxF3x0 series. In AT32F415 series, the external interrupts are configured through IOMUX_EXINTCx register, while in SxxF0xx/GxxF3x0 series, the configuration is done by SYSCFG_EXTICRx register. Only the mapping address of the EXTICRx registers have been changed, without any changes to the meaning of EXTIx configuration.

3.3.5 GPIO interface

Table 9.GPIO interface differences

GPIO	SXX32F0xx	GX32F3x0	AT32F415
Input mode	Floating PU PD	Floating PU PD	Floating PU PD
Output mode	PP PP+PU PP+PD OD OD+PU OD+PD	PP PP+PU PP+PD OD OD+PU OD+PD	PP OD
Alternate function	PP PP+PU PP+PD OD OD+PU OD+PD	PP PP+PU PP+PD OD OD+PU OD+PD	PP OD
Speed	2MHz 10MHz 48MHz	2MHz 10MHz 50MHz	GPIOx mode configuration (y=8~15) 00: Input mode (reset state) 01: Output mode, large sourcing/sinking strength 10: Output mode, normal sourcing/sinking strength 11: Output mode, normal sourcing/sinking strength sourcing/sinking strength

- **GPIO alternate function**

AT32F415:

1. The configuration of GPIO alternate function depends on the peripheral mode used. For example, USART Tx should be configured as an alternate function push-pull, while USART Rx should be configured as an input floating or an input pull-up.
2. To optimize the number of peripheral I/Os for different packages, it is possible to remap some alternate functions to other pins. The IOMUX_REMAPx register can be used to configure an I/O as an alternate function.

SXX32F0xx/GX32F3x0:

1. Whatever the peripheral mode used, the I/O must be configured as an alternate function, and then the I/O can be used in the proper way.
2. The configuration of the I/O alternate function and mapping can be done by GPIOx_AFRL and GPIOx_AFRH registers.

3.3.6 ADC interface

The table below presents the difference of ADC interface between AT32F415 series and SXX32F0xx/GX32F3x0 series:

Table 10. ADC differences

ADC	AT32F415		GX32F3x0		SXX32F0xx
Number of channels	16 channels+2 internal channels (No V_{BAT}/2)		16 channels +3 internal channels		16 channels +3 internal channels
Conversion Modes	Repetition/Split/Continuous/Preempted		Single/Continuous/ Discontinuous/Scan		Single/Continuous/ Discontinuous/Scan
Resolution	12-bit		12-bit		12-bit
External Trigger	Regular group TMR1 CH1 TMR1 CH2 TMR1 CH3 TMR2 CH2 TMR3 TRGOUT TMR4 CH4 EXINT line11 OCSWTRG TMR1_TRGOUT	Preempted group TMR1 TRGOUT TMR1 CH1 TMR1 CH4 TMR2 CH1 TMR2 TRGOUT TMR3 CH4 TMR4 TRGOUT EXINT line15 PCSWTRG	Regular group TMR1 CC1 TMR1 CC2 TMR1 CC3 TMR2 CC2 TMR3 TRGO TMR14 CC EXTI line11 SWSTR	Preempted group TMR1 TRGO TMR1 CC4 TMR2 TRGO TMR2 CC1 TMR3 CC4 TMR14 TRGO EXTI line15 JSWSTR	TIM 1_TRGO TIM 1_CC4 TIM 2_TRGO TIM 3_TRGO TIM 15_TRGO
Supply requirement	2.6 V to 3.6 V		2.6 V to 3.6 V		2.4 V to 3.6 V

3.3.7 SPI interface

- The SPI peripheral embedded in AT32F415 series is compatible with that of GX32F3x0 series
- The SPI interface has none of the following features versus the SXX32F0xx series:
  1. NSS pulse mode and TI mode
  2. Programmable data frame length
  3. Tx/Rx FIFO buffers

3.3.8 I2C interface

- The I2C peripheral embedded in AT32F415 series is compatible with that of GX32F3x0 series;
- There are big differences related to I2C versus SXX32F0xx.

The AT32F415 programming procedures, features and structure are different from those of the SXX32F0xx, so the code written for the SXX32F0xx series using the I2C needs to be rewritten to run on AT32F415 series.

3.3.9 USART interface

- The USART peripheral of the AT32F415 has big difference versus SXX32F0xx.

The AT32F415 programming procedures, features and structure are different from those of the SXX32F0xx, so the code written for the SXX32F0xx series using the USART needs to be rewritten to run on AT32F415 series.

3.3.10 Configure reference clock configuration table before enabling CRM PLL

- Due to the CRM IP update of AT32F415, it is necessary to configure the PLL_FR parameters in the reference clock configuration table according to the PLL clock source used before configuring and enabling CRM PLL (Register RCC_PLL [26:24]).

3.3.11 Internal temperature sensor

- The AT32F415 temperature sensor is compatible with GX32F3x0, but quite different from SXX32F0xx.

3.3.12 GPIO 5V-tolerant compatibility

- PA10, PA11, PA12, PD0 and PD1 are not 5V-tolerant input pins, so the input level of these pins should not exceed VDD + 0.3V.

3.3.13 ERTC calendar read

- AT32F415 is different from SXX32F0xx and GX32F3x0 in terms of reading the ERTC_TIME and ERTC_DATE registers. For AT32F415, it is necessary to read the ERTC_CTRL register first to update the time and data register values.

4 Revision history

Table 11. Document revision history

Date	Revision	Changes
2022.02.28	2.0.0	Initial release

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