MG0013
Migration Guide

Migrating from GX32F130 to AT32F421

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing GX32F130 series to AT32F421 series device. It puts together the most important information and lists the vital aspects that need to be taken into account.

To move an application from GX32F130 series to AT32F421 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F421xx

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1 Similarities and differences between AT32F421 and GX32F130

AT32F421 series microcontrollers are basically compatible with the GX32F130 series, and provide many enhanced features, some of which are different from GX32F130. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, define the alternate function of the pins
- Compiler tools: identical, for example, Keil, IAR

1.2 Overview of differences

Table 1. Differences between AT32F421 and GX32F130

	AT32F421	GX32F130xC/xB/x8
Core	Cortex-M4 (without FPU)	Cortex-M3
Voltage range	2.4 V~3.6 V	2.6 V~3.6 V
VBAT supply	Not support	Support
System clock	Max frequency 120 MHz, APB1 120 MHz, APB2 120 MHz	Max frequency 48 MHz, APB1 48 MHz, APB2 48 MHz
Boot Memory	4 KB, support Flash memory content CRC check	3 KB
Flash memory 16-bit write time	37 us	>200 us
Flash memory sector erase time	6.4 ms	100 ms
Flash memory mass erase time	8 ms	>3.2 s
SRAM size	8/16 KB by part number	4/8 KB by part number
SRAM parity check	NA	Support
GPIO locking	All GPIOs can be locked.	Only PA and PB can be locked.
PLL	Frequency multiplication factors from 31x to 500x; Frequency division factor from division by 1 to division by 15	Integer multiplication
I2S	2	NA
32-bit general-purpose timer	NA	TMR2
Basic timer	TMR6	NA
ADC	2 Msps (max ADCCLK = 28 MHz)	1 Msps (max ADCCLK = 14 MHz)
ESD parameters	HBM: 6 KV, CDM: 1000 V	HBM: 5 KV, CDM: 500 V
Run mode	7.62 mA@48 MHz	17.26 mA@48 MHz
Power consumption at Sleep mode	5.81 mA@48 MHz	9.76 mA@48 MHz
Power consumption	210 uA	143.17 uA

	AT32F421	GX32F130xC/xB/x8
at Deepsleep mode		
Power consumption at Standby mode	3.6 uA	5.74 uA
Temperature range	-40 to +105 °C	-40 to +85 °C
Packages	Up to LQFP48	Up to LQFP64

2 Hardware migration

The migration from GX32F130 to AT32F421 series is simple as because they are pin-to-pin compatible basically, with only a few pins being affected.

Table 2. Pin compatibility between AT32F421 and GX32F130

AT32F421					GX32F130				
TSSOP20	QFN28	QFN32	LQFP48	Pin name	TSSOP20	QFN28	QFN32	LQFP48	Pin name
-	-	-	1	VDD	-	-	-	1	VBAT

3 Software migration

3.1 Peripheral comparison

In terms of peripherals, there are some differences between AT32F421 and GX32F130, and some of them are new designs for AT32F421. Therefore, it is necessary to modify peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 3. Peripheral compatibility analysis

Peripheral	AT32F421	GX32F130	Compatibility	
			Pinout	Firmware driver
SPI	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Partial compatibility
DEBUG	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Partial compatibility
EXINT	Y	Y	Identical	Partial compatibility
DMA	Y	Y	NA	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
PWC	Y	Y	NA	Partial compatibility
USART	Y	Y	Identical	Incompatible
I2C	Y	Y	Identical	Partial compatibility
ADC	Y	Y	Identical	Partial compatibility
RTC	Y	Y	Identical	Partial compatibility
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	Identical	Partial compatibility
CMP	Y	NA	NA	NA
SCFG	Y	Y	Identical	Partial compatibility

3.2 Memory mapping

AT32F421 architecture is highly compatible with GX32F130, except the distribution of peripheral addresses and buses as shown in *Table 4*.

Table 4. Memory map differences

Peripheral	GX32F130		AT32F421	
	Bus	Base address	Bus	Base address
GPIOD		0x48000C00	NA	NA
DEBUG	APB2	0x40015800	CPU core	0xE0042000
TMR6	NA	NA	APB1	0x40001000
TMR2	APB1	0x40000000	NA	NA

3.3 Functional differences

This section describes the peripheral differences between AT32F421 and GX32F130.

3.3.1 CRM interface

- The differences related to CRM (Clock and reset management) in the AT32F421 series versus GX32F130 are presented in *Table 5*.

Table 5. CRM differences

CRM	GX32F130	AT32F421
HICK	8 MHz RC	48 MHz RC divided by 6
HEXT	4-32 MHz	4-25 MHz
HICK14	14 MHz RC ADC	NA
HICK48	NA	48 MHz RC
CLKOUT	HICK14, LICK, LEXT, HICK, HEXT, PLL, PLL/2	ADCCLK, SYSCLK, LICK, LEXT, HICK, HEXT, PLL/2, PLL/4

3.3.2 DMA interface

- The differences related to DMA in AT32F421 series versus GX32F130 are presented in *Table 6*.

Table 6. DMA differences

Peripheral	DMA request	GX32F130	AT32F421
TMR2	TMR2_UP TMR2_CH1 TMR2_CH2 TMR2_CH3 TMR2_CH4	DMA_Channel2 DMA_Channel5 DMA_Channel3 DMA_Channel1 DMA_Channel4	NA
TMR6	TMR6_UP	NA	DMA_Channel3
TMR15	TMR15_COM	NA	DMA_Channel5

3.3.3 Interrupt vectors

- *Table 7* presents the interrupt vectors and interrupt vector number in AT32F421 series versus GX32F130.

Table 7. Interrupt vector differences

Position	GX32F130	AT32F421
15	TMR2	Reserved
17	Reserved	TMR6
48	DMA_CH6_CH7	Reserved

3.3.4 GPIO interface

- The main difference related to GPIO between AT32F421 and GX32F130 is that the AT32F421 output mode does not support internal pull-up and pull-down.

Table 8. GPIO differences

GPIO	GX32F130	AT32F421
Output mode	PP PP+PU PP+PD OD OD+PU OD+PD	PP OD
Alternate function	PP PP+PU PP+PD OD OD+PU OD+PD	PP OD

3.3.5 ADC interface

- *Table 9* presents the differences related to ADC interface between AT32F421 series and GX32F130 series:

Table 9. ADC differences

ADC	GX32F130		AT32F421	
Number of channels	16 channels +3 internal channels		15 channels +3 internal channels (without V_{BAT} channel but with V_{SSA} channel)	
Clock	Dual clock domain (APB clock and HICK14 clock)		APB clock	
External Trigger	Regular group TMR2 CC2	Preempted group TMR2 TRGO TMR2 CC1	Regular group NA	Preempted group NA NA
Supply requirement	2.6 V to 3.6 V		2.4 V to 3.6 V	

3.3.6 USART interface

The USART peripheral of the AT32F421 has big difference versus GX32F130. The AT32F421 programming procedures, features and structure are different from those of the GX32F130, so the code written for the GX32F130 series using the USART needs to be rewritten to run on AT32F421 series.

3.3.7 CRM PLL

- For AT32F421, it is necessary to configure the PLL_FREF parameters (CRM_PLL[26:24]) in the reference configuration table according to the PLL clock source used before programming and enabling CRM PLL.

3.3.8 FLASH interface

- The Flash memory differences between AT32F421 and GX32F130 are shown in *Table 10*.

Table 10. Flash memory differences

SYSCLK Range	GX32F130	AT32F421
0 MHz < SYSCLK <= 32 MHz	NA	Zero wait
32 MHz < SYSCLK <= 64 MHz		One wait
64 MHz < SYSCLK <= 96 MHz		Two waits
96 MHz < SYSCLK <= 120 MHz		Three waits

3.3.9 RTC interface

- AT32F421 only supports tamper detection 0 (tamper0), not tamper 1, compared to GX32F130.

3.3.10 PWC

- Additional PB5 (WKUP6) and PB15 (WKUP7) are used as wakeup pins in AT32F421 versus GX32F130
- Extra low-power mode of internal voltage regulator in Deepsleep mode is supported in AT32F421 versus GX32F130

3.4 Functional enhancement

This section describes the enhanced peripheral features of AT32F421 versus GX32F130.

3.4.1 High frequency PLL settings

- AT32F421 embeds a PLL that can output up to 120 MHz clock, with slight different settings.

3.4.2 AT32F421 PLL prescaler

- Prescaler is extended due to its max frequency up to 120 MHz
- ADC prescaler supports /12, /16 output

3.4.3 Security library (sLib)

- Security library (sLib) feature is provided to prevent important IP-code from being modified or read by end applications so as to enhance security level.

3.4.4 GPIO 5V-tolerant compatibility

- AT32F421 provides more 5V-tolerant input pins compared to GX32F130, except PC14, PC15, PF0 and PF1 (the input level of these pins should not exceed VDD + 0.3V).
- All other pins are 5V-tolerant.

4 Revision history

Table 11. Document revision history

Date	Revision	Changes
2022.02.25	2.0.0	Initial release
2022.05.30	2.0.1	Deleted the description “PWC enters low-power mode through WFE”
2022.10.17	2.0.2	Added *3.3.10 PWC*