MG0019
Migration Guide

Migrating from AT32F415 to AT32F425

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing AT32F415 series to AT32F425 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from AT32F415 series to AT32F425 series, users have to analyze the hardware and software migration.

Applicable products：

Part numbers	AT32F425xx

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1 Similarities and differences between AT32F425 and AT32F415

AT32F425 series microcontrollers are basically compatible with the AT32F415 series, and provide many enhanced features, some of which are different from AT32F415. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, the alternate functions of pins are defined
- Compiler tools: identical, for example, Keil, IAR.

1.2 Overview of differences

Table 1. Differences between AT32F425 and AT32F415

	AT32F425	AT32F415
System clock	Max frequency 96 MHz, APB1 96 MHz, APB2 96 MHz	Max frequency 150 MHz, APB1 75 MHz, APB2 75 MHz
Startup	3.5 ms	0.6 ms
Wake up from Deepsleep mode (Voltage regulator is in low-power mode)	450 us	360 us
Wake up from Standby mode	800 us	600 us
Flash size	16/32/64 KB	64/128/256 KB
SRAM size	20 KB	32 KB
16-bit timer	7	6
32-bit timer	1	2
Basic timer	2	-
ACC	Support	-
CMP	-	2
SDIO	-	1
USART	USART4 (with synchronous communication support)	UART4 (without synchronous communication support)
Internal temperature sensor	-	Support
Comparator	-	2
OTG device endpoint	8 x IN, 8 x OUT (include endpoint 0)	4 x IN, 4 x OUT (include endpoint 0)
Number of OTG master channels	16	8
Operating supply	2.4 V~3.6 V	2.6 V~3.6 V

	AT32F425	AT32F415
ESD	HBM: 6 KV, CDM: 2 KV	HBM: 5 KV, CDM: 1 KV
Typical current in Run mode	13.5mA@72Mhz with all peripherals enabled	24.6mA@72Mhz with all peripherals enabled
Typical current in Sleep mode	10.8mA@72Mhz with all peripherals enabled	19mA@72Mhz with all peripherals enabled
Typical current in Deepsleep mode (LDO is in low-power mode)	123 uA	680 uA
Typical current in Standby mode	5.0 uA	6.6 uA

2 Hardware migration

AT32F425 series is pin-to-pin compatible with AT32F415 series for the same packages. As they differ in the GPIO peripheral, it is necessary to refer to the corresponding Datasheet for more information on the peripheral functions of each pin.

Table 2. Peripheral compatibility analysis

AT32F425					AT32F415				
LQFP64	LQFP48	QFN48	QFN32	Pin name	LQFP64	LQFP48	QFN48	QFN32	Pin name
1	1	1	1	Vdd	1	1	1	1	Vbat
5	5	5	2	PF0	5	5	5	2	PD0
6	6	6	3	PF1	6	6	6	3	PD1

3 Boot mode compatibility

In most cases, AT32F425 and AT32F415 series load a Boot mode on a system reset. However, for AT32F425 series, if embedded SRAM Boot mode is selected, the BOOT status is then locked. In this case, it is impossible to load a new Boot mode on a system reset unless a power-on reset occurs.

AT32F415 series observes the configuration of the Boot mode selection in *Table 3*. The BOOT0 and BOOT1 state correspond to the level on the BOOT0 and BOOT1 pins respectively.

Table 3. AT32F415 Boot mode

Boot mode selection		Boot modes	Description
BOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	Boot memory	Boot memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

AT32F425 series observes the configuration of the Boot mode selection in *Table 4*. BOOT0 state corresponds to the level on the BOOT0 pin, while the nBOOT1 corresponds to the nBOOT1 bit value of the system configuration byte (SSB) within the User System Data (USD).

Table 4. AT32F425 Boot mode

Boot mode selection		Boot modes	Description
nBOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
1	1	Boot memory	Boot memory is selected as boot space
0	1	Embedded SRAM	Embedded SRAM is selected as boot space

4 Software migration

4.1 Peripheral comparison

AT32F425 series is mostly compatible with AT32F415 series in terms of peripherals, except for a few function enhancements or new designs. Thus it is necessary to modify these peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 5. Peripheral compatibility analysis

Peripheral	AT32F425	AT32F415	Compatibility	
			Pinout	Firmware driver
PWC	Y	Y	NA	Partial compatibility
CRM	Y	Y	Identical	Partial compatibility
CMP	NA	Y	NA	Incompatible
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	Identical	Incompatible
IOMUX	NA	Y	NA	Incompatible
SCFG	Y	NA	NA	Incompatible
EXINT	Y	Y	Identical	Partial compatibility
DMA	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Full compatibility
I2C	Y	Y	Identical	Incompatible
USART	Y	Y	Identical	Partial compatibility
SPI	Y	Y	Identical	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Full compatibility
RTC	Y	Y	Identical	Partial compatibility
ADC	Y	Y	Identical	Partial compatibility
CAN	Y	Y	Identical	Partial compatibility
OTGFS	Y	Y	Identical	Partial compatibility
ACC	Y	NA	NA	Incompatible
IRTMR	Y	NA	NA	Incompatible
SDIO	NA	Y	NA	Incompatible
DEBUG	Y	Y	NA	Incompatible

4.2 Functional differences

This section describes the peripheral differences in the AT32F425 series versus AT32F415 series. The peripheral behavior of the AT32F425 series is detailed in the subsections below.

4.2.1 Memory mapping

- *Table 6* presents the differences related to address mapping and bus distribution in AT32F425 versus AT32F415.

Table 6. Memory map differences

Peripheral	AT32F425		AT32F415	
	Bus	Base address	Bus	Base address
GPIOF	AHB	0x48001400	AHB	0x40011C00
GPIOD		0x48000C00		0x40011400
GPIOC		0x48000800		0x40011000
GPIOB		0x48000400		0x40010C00
GPIOA		0x48000000		0x40010800
DMA2	N/A	N/A		0x40020400
SDIO1	N/A	N/A		0x40018000
TMR11	N/A	N/A	APB2	0x40015400
TMR10				0x40015000
TMR9				0x40014C00
TMR17	APB2	0x40014800	N/A	N/A
TMR16		0x40014400		
TMR15		0x40014000		
SCFG		0x40010000		
IOMUX	N/A	N/A	APB2	0x40010000
ACC	APB1	0x40006C00	N/A	N/A
UART5	N/A	N/A	APB1	0x40005000
SPI3	APB1	0x40003C00	N/A	N/A
CMP	N/A	N/A	APB1	0x40002400
TMR14	APB1	0x40002000	N/A	N/A
TMR13		0x40001C00		
TMR7		0x40001400		
TMR6		0x40001000		
TMR5	N/A	N/A	APB1	0x40000C00
TMR4				0x40000800

4.2.2 Flash interface

- *Table 7* presents the differences between AT32F425 series and AT32F415 in terms of Boot memory and User System Data area.

Table 7. Flash memory address differences

Memory	AT32F425	AT32F415
Boot memory	0x1FFFE400-0x1FFFF3FF	0x1FFFAC00-0x1FFFF3FF
User System Data area	0x1FFFF800-0x1FFFF9FF	0x1FFFF800-0x1FFFFBFF

4.2.3 Interrupt vectors

- *Table 8* presents the interrupt vector differences in AT32F425 series versus AT32F415 series.

Table 8. Interrupt vector differences

Position	AT32F425	AT32F415
0	WWDT	WWDT
1	PVM	PVM
2	ERTC	TAMPER
3	FLASH	ERTC
4	CRM	FLASH
5	EXINT1_0	CRM
6	EXINT3_2	EXINT0
7	EXINT15_4	EXINT1
8	ACC	EXINT2
9	DMA1_CH1	EXINT3
10	DMA1_CH3_2	EXINT4
11	DMA1_CH7_4	DMA1_CH1
12	ADC1	DMA1_CH2
13	TMR1_BRK_OVF_TRG_HALL	DMA1_CH3
14	TMR1_CH	DMA1_CH4
15	TMR2	DMA1_CH5
16	TMR3	DMA1_CH6
17	TMR6	DMA1_CH7
18	TMR7	ADC1
19	TMR14	CAN1_TX
20	TMR15	CAN1_RX0
21	TMR16	CAN1_RX1
22	TMR17	CAN1_SE
23	I2C1_EVT	EXINT9_5
24	I2C2_EVT	TMR1_BRK_TMR9
25	SPI1	TMR1_OVF_TMR10
26	SPI2	TMR1_TRG_HALL_TMR11
27	USART1	TMR1_CH
28	USART2	TMR2
29	USART4_3	TMR3
30	CAN1	TMR4
31	OTGFS1	I2C1_EVT
32	I2C1_ERR	I2C1_ERR
33	SPI3	I2C2_EVT
34	I2C2_ERR	I2C2_ERR
35	TMR13	SPI1
36	Reserved	SPI2
37	Reserved	USART1
38	Reserved	USART2
39	Reserved	USART3

Position	AT32F425	AT32F415
40	Reserved	EXINT15_10
41	Reserved	ERTCAlarm
42	Reserved	OTGFS1_WKUP
43	Reserved	Reserved
44	Reserved	Reserved
45	Reserved	Reserved
46	Reserved	Reserved
47	Reserved	Reserved
48	Reserved	Reserved
49	Reserved	SDIO1
50	Reserved	TMR5
51	Reserved	Reserved
52	Reserved	UART4
53	Reserved	UART5
54	Reserved	Reserved
55	Reserved	Reserved
56	Reserved	DMA2_CH1
57	Reserved	DMA2_CH2
58	Reserved	DMA2_CH3
59	Reserved	DMA2_CH5_4
60	Reserved	Reserved
61	Reserved	Reserved
62	Reserved	Reserved
63	Reserved	Reserved
64	Reserved	Reserved
65	Reserved	Reserved
66	Reserved	Reserved
67	Reserved	OTGFS1
68	Reserved	Reserved
69	Reserved	Reserved
70	Reserved	CMP1
71	Reserved	CMP2
72	Reserved	Reserved
73	Reserved	Reserved
74	Reserved	Reserved
75	Reserved	DMA2_CH7_6

4.2.4 DMA interface

- AT32F425 series has only one DMA controller (DMA1), while the AT32F415 series has two DMA controllers (DMA1 and DMA2)
- AT32F425 series supports DMA flexible mapping mode, while the AT32F415 series contain two DMA mapping mode, fixed mapping and flexible ones.

4.2.5 PWC interface

Table 9. PWC interface differences

PWR	AT32F425	AT32F415
Wake-up pin from Standby mode	6 x WKUP pins	1 x WKUP pin
Internal voltage regulator	Support extra low-power mode of the internal voltage regulator in Deepsleep mode.	Not support

- *Table 9* presents the differences between the PWR interface of the AT32F425 series and AT32F415 series. The AT32F425 series adds more WKUP pins from Standby mode in order to adapt to more application scenarios, compared to AT32F415. In addition, AT32F425 series allows to enable extra low-power mode of the internal voltage regulator in Deepsleep mode. This feature is useful to further reduce power consumption when Deepsleep mode is enabled.

4.2.6 ADC interface

- AT32F425 series embeds an enhanced ADC peripheral compared to AT32F415 series. *Table 10* presents the differences of ADC interface.

Table 10. ADC interface differences

ADC	AT32F425		AT32F415	
Channel	ADC_IN16 refers to Vssa		ADC_IN16 refers to as internal temperature sensor	
Oversampling	2 to 256 times hardware oversampling		Not support	
External trigger	Regular group TMR1_TRGOUT TMR1_CH4 TMR2_TRGOUT TMR3_TRGOUT TMR15_TRGOUT TMR1_CH1 EXINT_Line11 OCSWTRG	Preempted group TMR1_CH2 TMR1_CH3 TMR2_CH4 TMR3_CH4 TMR15_CH1 TMR6_TRGOUT EXINT_Line15 PCSWTRG	Regular group TMR1_CH1 TMR1_CH2 TMR1_CH3 TMR2_CH2 TMR3_TRGOUT TMR4_CH4 EXINT_Line11 TMR1_TRGOUT OCSWTRG TMR1_TRGOUT	Preempted group TMR1_TRGOUT TMR1_CH4 TMR2_TRGOUT TMR2_CH1 TMR3_CH4 TMR4_TRGOUT EXINT_Line15 TMR1_CH4 PCSWTRG TRM1_CH1

4.2.7 EXINT interrupt source selection

- There are some differences between the external interrupt configuration mode of the AT32F425 series and AT32F415 series. The AT32F415 series uses the IOMUX_EXINTCx register to configure external interrupts, while AT32F425 series uses the SYSCFG_EXTICRx register. In this way, only the mapping address of the EXTICRx register has changed, without any change to the meaning of EXTIx configuration

4.2.8 GPIO interface

- The differences related to GPIO peripheral in the AT32F425 series versus AT32F415 series are described as follows:

  AT32F425:

  AT32F425 series GPIOs are configured through three registers, GPIOx_CFGR register (configure IO operating mode), GPIOx_OMODE register (configure output mode) and GPIOx_PULL register (configure IO pull-up/pull-down). The IO pull-up/pull-down configurations apply to the general-purpose input/output mode and alternate function mode.

  AT32F415:

  AT32F415 series GPIOs are configured through two registers, GPIOx_CFGLR and GPIOx_CFGHR. These registers can be used to configure IO operating mode, output mode and IO pull-up/pull-down mode. The IO pull-up/pull-down configurations apply to the input mode.

4.2.9 IOMUX

- The differences related to IOMUX peripheral in the AT32F425 series versus AT32F415 series are described as follows:

  AT32F425:

  For AT32F425 series, it is required that the I/O pin is configured as alternate function for peripherals to use I/O functions properly.

  Pin multiplexing and mapping are configured through the GPIOx_MUXL and GPIOx_MUXH registers.

  AT32F415:

  I/O alternate function configuration depends on the peripheral mode used. For instance, the USART Tx pin should be configured as alternate function push-pull, and the USART Rx should be input floating or input pull-up.

  To optimize the number of peripheral I/O functions on different packages, it is possible to remap some alternate functions to other pins. The IOMUX_REMAPx register is used to configure the alternate functions of the peripheral pins.

4.2.10 ERTC interface

- There are no big differences related to ERTC peripheral in AT32F425 versus AT32F415, except only a slight change (AT32F415 has alarm B feature).

4.2.11 SPI interface

- AT32F425 series has additional features compared to AT32F415 series:

  1. TI mode

  This mode is enabled through the TIEN control bit within the SPI_CTRL2 register.

  2. I2S full-duplex mode

  This mode is configured through the I2S_FD control bit within the SCFG_CFG2 register.

4.2.12 I²C interface

- AT32F425 series I2C peripheral is different from that of AT32F415 series. They are incompatible in software.

4.2.13 USART interface

- In addition to the original features, AT32F425 series provides additional features compared to AT32F415 series:
  1. TX/RX SWAP feature
  2. RS485 communication mode
  3. 7-bit data length mode

4.2.14 Security library interface

- The security library of the AT32F425 series is optimized compared to the AT32F415, with slight differences.

4.2.15 TMR interface

- In TMR peripheral, AT32F425 adds the description of the channel 5 of TMR1 (advanced timer), including two registers of TMRx_CM3 and TMRx_C5DT, channel interrupt, flag and other bits
- In TMR peripheral, AT32F425 supports TMR1 (advanced timer) TRGOUT2 output feature. This feature is enabled through the TRGOUT2EN bit in the TMRx_CTRL2 register
- In AT32F425, the repetition register (TMRx_RPR) of TMR1 (advanced timer) is expanded to be 16-bit register
- In TMR peripheral, AT32F425 supports break input filtering feature for TMR1/15/16/17 timers. This can be configured through the BKF bit in the TMRx_ BRK register

4.2.16 WDT interface

- AT32F425 adds window feature for WDT peripheral, and supports stoping counting in Deepsleep and Standby modes, with other functions being the same as those of AT32F415 and software compatible. The AT32F425 is downward compatible with AT32F415.

4.3 Peripheral enhancement

4.3.1 AT32F425 additional WKUP pins

- Apart from retaining the original WKUP pin (WKUP1-PA0) used in AT32F415, the AT32F425 series provides additional five WKUP pins from Standby mode.

  WKUP pin 2——PC13

  WKUP pin 4——PA2

  WKUP pin 5——PC5

  WKUP pin 6——PB5

  WKUP pin 7——PB15

  These five WKUP pins have their respective enable bits (refer to the corresponding datasheet and technical manual for more information). When enabled, the wake-up event on the corresponding pin can wake up from Standby mode. It is possible to enable one or more wake-ups pins to wake up from Standby mode according to the actual application requirements.

4.3.2 AT32F425 infrared transmitter

- This infrared transmitter is based on the internal connection between TMR16 and USART1, or USART4 and TMR17. The TMR17 is used to provide carrier frequency, while the TMR16, USART1 or USART4 provides the main signals to be sent. The infrared output signal is available on PB9 or PA13.

4.3.3 AT32F425 TMR 16-bit RPR register

- The RPR (repetition period) register of the TMR is increased from 8-bit to 16-bit. In single-pulse mode, it is possible to configure RPR register to achieve multi-pulse function, which can send up to 65536 pulses at once.

4.3.4 AT32F425 HICK auto clock calibration module

- HICK auto clock calibration (ACC) uses the SOF signal (1 ms period) coming from the USB module as a reference signal to perform HICK clock sampling and calibration. This feature is mainly used to provide the USB device with 48 MHz±0.25% accuracy clock.

4.3.5 AT32F425 OTGFS device endpoint and master channel

- In device mode, OTGFS supports one bidirectional control endpoint, seven IN endpoints and seven OUT endpoints.
- In master mode, OTGFS supports 16 master channels.

5 Revision history

Table 11. Document revision history

Date	Revision	Changes
2021.12.6	2.0.0	Initial release
2022.1.11	2.0.1	Updated the document format, and added OTGFS differences.
2022.10.19	2.0.2	Added *4.2.15 TMR interface* Added *4.2.16 WDT interface*

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