MG0021
Migration Guide

Migrating from AT32F421 to AT32L021

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing AT32F421 series to AT32L021 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from AT32F421 series to AT32L021 series, users have to analyze the hardware and software migration.

Applicable products:

Part number	AT32L021xx

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1 Similarities and differences between AT32L021 and AT32F421

AT32L021 series microcontrollers are basically compatible with the AT32F421 series, and improve performances such as lower power consumption, and some of which are different from AT32F421. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, define the alternate functions of the pins.
- Compiler tools: identical, for example, Keil and IAR.

1.2 Overview of differences

Table 1. Differences between AT32F421 and AT32L021

	AT32L021	AT32F421
Core	Cortex-M0+	Cortex-M4 (without FPU)
Hardware division	Dedicated hardware divider	Cortex-M4 core
Voltage range	1.71 V~3.6 V	2.4 V~3.6 V
System clock	Max. frequency 80 MHz, APB1 80 MHz, APB2 80 MHz	Max. frequency 120 MHz, APB1 120 MHz, APB2 120 MHz
SRAM size	All 8 KB, extendable up to 9 KB	8/16 KB by part number
SRAM parity check	Support	NA
GPIO controller	Dedicated GPIO bus	AHB bus
CAN	1	NA
USART	4	2
IRTMR	Signals not from USART	Signals selected from USART1 and USART2
Comparator (CMP)	NA	1
Temperature sensor	NA	Support
I^2C wakeup from Deepsleep mode	Support	Not support
USART wakeup from Deepsleep mode	Support USART1 and USART2	Not support
Wake up from Deepsleep mode	17us	450 us
Wake up from Standby mode	72us	1250 us
Run mode	12.7 mA@80 MHz	10.5 mA@72 MHz
Power consumption in Sleep mode	10.2 mA@80 MHz	7.76 mA@72 MHz

	AT32L021	AT32F421
Power consumption in Deepsleep mode	9.24 uA	210 uA
Power consumption in Standby mode	1.24 uA	3.6 uA
WDT stops counting in low-power mode	Support	Not support
Packages	Support QFN20	Not support QFN20

2 Hardware migration

The migration from AT32F421 to AT32L021 series is simple as they are pin-to-pin compatible for the same packages.

3 Software migration

3.1 Peripheral comparison

There are some differences between AT32L021 and AT32F421 in terms of peripherals, some of which are new designs for AT32L021 series. Therefore, it is necessary to modify these peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 2. Peripheral compatibility analysis

Peripheral	AT32L021	AT32F421	Compatibility	
			Pinout	Firmware driver
SPI	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Partial compatibility
DEBUG	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Full compatibility
EXINT	Y	Y	Identical	Full compatibility
DMA	Y	Y	NA	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
PWC	Y	Y	NA	Partial compatibility
USART	Y	Y	Identical	Partial compatibility
I^2C	Y	Y	Identical	Incompatible
ADC	Y	Y	Identical	Partial compatibility
RTC	Y	Y	Identical	Full compatibility
FLASH	Y	Y	NA	Full compatibility
GPIO	Y	Y	Identical	Partial compatibility
CMP	NA	Y	NA	Incompatible
CAN	Y	NA	NA	Incompatible
HWDIV	Y	NA	NA	Incompatible
SCFG	Y	Y	Identical	Partial compatibility
IRTMR	Y	Y	Identical	Full compatibility

3.2 Memory mapping

AT32L021 architecture is highly compatible with AT32F421, except the distribution of peripheral addresses and buses as shown in Table 3.

Table 3. Memory map differences

Peripheral	AT32L021		AT32F421	
	Bus	Base address	Bus	Base address
HWDIV	AHB	0x40030000	NA	NA
DEBUG	APB2	0x40015800	CPU core	0xE0042000
CMP	NA	NA	APB2	0x40010000
CAN	APB1	0x40006400	NA	NA
USART4		0x40004C00		
USART3		0x40004800		

3.3 Functional differences

This section describes the peripheral differences between AT32L021 and AT32F421.

3.3.1 CRM

- HICKCAL (high speed internal clock calibration): CRM_CTRL[13:8] of AT32L021; CRM_CTRL[15:8] of AT32F421
- HICKTRIM (high speed internal clock trimming): CRM_CTRL[4:2] of AT32L021; CRM_CTRL[7:2] of AT32F421
- I^2C1/USART1/USART2 clock source: configurable in AT32L021 series; APB bus clock (fixed) in AT32F421 series.

3.3.2 DMA

- The difference related to DMA in AT32L021 series versus AT32F421 series is the DMA request mapping. AT32F421 supports fixed DMA request mapping, which means that each peripheral has a fixed DMA channel to manage requests, while AT32L021 supports flexible DMA request mapping, which makes DMA channel configuration more flexible.

3.3.3 GPIO

- Dedicated GPIO bus in the AT32L021 series, AHB not shared, to increase efficiency
- GPIO 5 V-tolerant pin compatibility

  AT32L021 series provides more 5V-tolerant pins. PC14 and PC15 are not 5V-tolerant, and their input level is not greater than V_{DD} + 0.3 V.

  For greater flexibility, FTa pin of the AT32L021 series is always 5 V-tolerant except when ADC is enabled and conversion on this pin is enabled.
- AT32L021 series supports internal pull-up/pull-down in output mode, and it is designed with a TOGR register to toggle the corresponding I/O quickly.

Table 4. GPIO pull-up/pull-down configuration differences

GPIO	AT32L021	AT32F421
Output mode	PP	PP
	PP + PU	Not support
	PP + PD	Not support
	OD	OD
	OD + PU	Not support
	OD + PD	Not support
Multiplexed function	PP	PP
	PP + PU	Not support
	PP + PD	Not support
	OD	OD
	OD + PU	Not support
	OD + PD	Not support

- AT32L021 series has two additional FTf pins with 20 mA sinking strength, and its I^2C bus supports enhanced fast mode.

3.3.4 ADC

- The differences related to ADC in AT32L021 series versus AT32F421 series are listed in Table 5.

Table 5. ADC differences

ADC	AT32L021	AT32F421
Resolution	6/8/10/12-bit	Fixed 12-bit
Oversampling	Hardware oversampling	Software oversampling
Precharge	Support	Not support
Temperature sensor	No internal temperature sensor	With an internal temperature sensor

3.3.5 USART

- The AT32L021 series embeds a USART peripheral, which inherits USART features of AT32F421 series and further extends functions including:
  1. Configurable clock domain for USART1 and USART2 (selected from PCLK, SYSCLK, HICK and LEXT); support Deepsleep wakeup when HICK or LEXT is used as the clock source
  2. Hardware RS485 mode
  3. Programmable data word length: 7/8/9 bits for AT32L021, while 8/9 bits for AT32F421
  4. Programmable data transmission order (MSB/LSB)
  5. Programmable Tx/Rx pin polarity
  6. Programmable DT polarity
  7. Modbus related functions (receiver time out & character match)

3.3.6 I^2C

- There are big differences between the I^2C interfaces of AT32L021 versus AT32F421. The architecture, features and programming interface are different. Therefore, any code written for the AT32F421 series using the I^2C needs to be rewritten to run on the AT32L021 series.
- For the AT32L021 series, clock domain of I^2C1 can be selected from PCLK, SYSCLK and HICK. When HICK is used as the clock source, waking up from Deepsleep mode is supported.

3.3.7 WDT

- The WDT of AT32L021 series can stop counting in Standby mode and Deepsleep mode.

3.3.8 SPI

- The SPI interface of AT32L021 series adds the following features compared to that of the AT32F421 series:
  1. PCLK/3 for SPI clock
  2. Compatible with the TI protocol
  3. CS pulse abnormal setting flag in TI slave mode

3.3.9 PWC

- The PWC of AT32L021 series adds the following features compared to that of the AT32F421 series:
  1. LDO voltage regulation
  2. Add WKUP4 pin
  3. Not support LDO extra low-power mode in Deepsleep mode
  4. PVM threshold (refer to Datasheet)

3.3.10 TMR

- The AT32L021 series supports TMR brake function.
- The AT32L021 series adds channel 5 and TRGOUT2 enable bit.

3.3.11 SCFG

- The SCFG of AT32L021 series can be used to connects the following signals to TMR brake input:
  1. PVM interrupt lock and PWM interrupt connects to TMR1/15/16/17 brake input
  2. SRAM odd parity check error connects to TMR1/15/16/17 brake input
  3. Cortex®-M0+ LOCKUP output connects to TMR1/15/16/17 brake input

3.4 Peripheral enhancement

This section introduces enhanced peripherals of AT32L021 series.

3.4.1 CAN

- The AT32L021 series has one CAN interface (2.0B Active), with 256 bytes of dedicated SRAM.

3.4.2 USART

- Add USART3 and USART4.

4 Revision history

Table 6. Document revision history

Date	Version	Revision note
2024.01.25	2.0.0	Initial release.

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