**MG0023**
Migration Guide

Migrating from AT32F415 to AT32F423

# Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing AT32F415 series to AT32F423 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from AT32F415 series to AT32F423 series, users have to analyze the hardware and software migration.

Applicable products：

| Product series | AT32F423xx |
|---|---|

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# 1 Similarities and differences between AT32F423 and AT32F415

AT32F423 series microcontrollers are generally compatible with the AT32F415 series except for some of its optimized peripherals that are not compatible by software. The differences between them are detailed in this document.

## 1.1 Overview of similarities

- Pin definition: The same packages have the same pin definitions. For extended peripherals, the alternate functions of the pins are defined.
- Compiler tools: identical, such as Keil, IAR, AT32 IDE

## 1.2 Overview of differences

**Table 1. Differences between AT32F423 and AT32F415**

| | AT32F423 | AT32F415 |
|---|---|---|
| System clock | Max frequency 150 MHz, APB1 120 MHz, APB2 150 MHz | Max frequency 150 MHz, APB1 75 MHz, APB2 75 MHz |
| FPU (Floating point unit ) | Support | Not support |
| Wake up from Deepsleep mode (LDO is in low-power mode) | 500 us | 360 us |
| Wake up from Standby mode | 800 us | 600 us |
| SRAM size | 32/48 KB | 32 KB |
| Bootloader | 20 KB, support USART3 | 18 KB |
| 16-bit timer | 8 | 6 |
| 32-bit timer | 1 | 2 |
| Basic timer | 2 | - |
| ACC | Support | - |
| CMP | - | 2 |
| ADC | 5.33 MSPS, 27 channels | 2 MSPS, 16 channels |
| DAC | 2 channels | - |
| DMA | Support DMAMUX | Not support DMAMUX |
| CAN | 2 | 1 |
| SPI/I2S | 3 | 2 |
| SDIO | - | 1 |
| USART | 8 | 5 |

| | AT32F423 | AT32F415 |
|---|---|---|
| XMC | Support | - |
| OTG device endpoint | 8 x IN, 8 x OUT (include endpoint 0) | 4 x IN, 4 x OUT (include endpoint 0) |
| Number of OTG host channels | 16 | 8 |
| Operating supply | 2.4 V~3.6 V | 2.6 V~3.6 V |
| $V_{BAT}$ | - | Support |
| Typical current in Run mode | 20.4 mA@72Mhz<br>with all peripherals enabled | 24.6 mA@72Mhz with all peripherals enabled |
| Typical current in Sleep mode | 16.5 mA@72Mhz with all peripherals enabled | 19mA@72Mhz with all peripherals enabled |
| Typical current in Deepsleep mode (LDO is in low-power mode) | 143 uA | 680 uA |
| Typical current in Standby mode | 5.4 uA | 6.6 uA |
| Package | Max. LQFP100, introduce QFN36 | Max. LQFP64 |

# 2 Hardware migration

AT32F423 series is generally pin-to-pin compatible with AT32F415 series for the same packages. As they differ in GPIO peripherals, it is necessary to refer to the corresponding Datasheet for more information on the peripheral functions of each pin.

**Table 2. Pinout comparison**

| AT32F423 series | | | | | AT32F415 series | | | | |
|---|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP48 | QFN48 | QFN32 | Pin name | LQFP64 | LQFP48 | QFN48 | QFN32 | Pin name |
| 5 | 5 | 5 | 2 | PF0 | 5 | 5 | 5 | 2 | PD0 |
| 6 | 6 | 6 | 3 | PF1 | 6 | 6 | 6 | 3 | PD1 |
| 18 | - | - | - | Vss | 18 | - | - | - | PF4 |
| 19 | - | - | - | Vdd | 19 | - | - | - | PF5 |
| 31 | 23 | 23 | - | PF8 | 31 | 23 | 23 | - | Vss |
| 48 | 36 | 36 | - | Vdd | 48 | 36 | 36 | - | PF7 |

# 3 Boot mode compatibility

In most cases, AT32F423 and AT32F415 series load a Boot mode on a system reset. However, for AT32F423 series, if embedded SRAM Boot mode is selected, the BOOT status is then locked. In this case, it is impossible to load a new Boot mode on a system reset unless a power-on reset occurs.

AT32F415 series observes the configuration of the Boot mode selection in *Table 3*. The BOOT0 and BOOT1 state correspond to the level on the BOOT0 and BOOT1 pins respectively.

**Table 3. AT32F415 Boot mode**

| Boot mode selection | | Boot modes | Description |
|---|---|---|---|
| BOOT1 | BOOT0 | | |
| X | 0 | Main Flash memory | Main Flash memory is selected as boot space |
| 0 | 1 | Boot memory | Boot memory is selected as boot space |
| 1 | 1 | Embedded SRAM | Embedded SRAM is selected as boot space |

AT32F423 series observes the configuration of the Boot mode selection in *Table 4*. BOOT0 state corresponds to the level on the BOOT0 pin, while the nBOOT1 corresponds to the nBOOT1 bit value of the system configuration byte (SSB) within the User System Data (USD).

**Table 4. AT32F423 Boot mode**

| Boot mode selection | | Boot modes | Description |
|---|---|---|---|
| nBOOT1 | BOOT0 | | |
| X | 0 | Main Flash memory | Main Flash memory is selected as boot space |
| 1 | 1 | Boot memory | Boot memory is selected as boot space |
| 0 | 1 | Embedded SRAM | Embedded SRAM is selected as boot space |

# 4 Software migration

## 4.1 Peripheral comparison

AT32F423 series is generally compatible with AT32F415 series in terms of peripherals, except for a few function enhancements or new designs. Thus it is necessary to modify these peripherals or use new peripheral drivers for brand-new design during the application-level program development.

**Table 5. Peripheral compatibility analysis**

| Peripheral | AT32F423 | AT32F415 | Compatibility | |
|---|---|---|---|---|
| | | | Pinout | Firmware driver |
| PWC | Y | Y | NA | Partial compatibility |
| CRM | Y | Y | Identical | Partial compatibility |
| CMP | NA | Y | NA | Incompatible |
| FLASH | Y | Y | NA | Partial compatibility |
| GPIO | Y | Y | Identical | Incompatible |
| IOMUX | NA | Y | NA | Incompatible |
| SCFG | Y | NA | NA | Incompatible |
| EXINT | Y | Y | Identical | Partial compatibility |
| DMA | Y | Y | NA | Partial compatibility |
| CRC | Y | Y | NA | Full compatibility |
| I2C | Y | Y | Identical | Incompatible |
| USART | Y | Y | Identical | Partial compatibility |
| SPI | Y | Y | Identical | Partial compatibility |
| TMR | Y | Y | Identical | Partial compatibility |
| WWDT | Y | Y | NA | Full compatibility |
| WDT | Y | Y | NA | Full compatibility |
| RTC | Y | Y | Identical | Partial compatibility |
| ADC | Y | Y | Identical | Incompatible |
| DAC | Y | NA | NA | Incompatible |
| CAN | Y | Y | Identical | Full compatibility |
| OTGFS | Y | Y | Identical | Partial compatibility |
| ACC | Y | NA | NA | Incompatible |
| IRTMR | Y | NA | NA | Incompatible |
| SDIO | NA | Y | NA | Incompatible |
| DEBUG | Y | Y | NA | Incompatible |
| XMC | Y | NA | NA | Incompatible |

## 4.2 Functional differences

This section describes the peripheral differences in the AT32F423 series versus AT32F415 series. The peripheral behavior of the AT32F423 series is detailed in the subsections below.

### 4.2.1 Memory mapping

- *Table 6* presents the differences related to address mapping and bus distribution in AT32F423 versus AT32F415.

**Table 6. Memory map differences**

| Peripheral | AT32F423 | | AT32F415 | |
|---|---|---|---|---|
| | Bus | Base address | Bus | Base address |
| XMC | AHB | 0xA0000000 | N/A | N/A |
| DMA2 | | 0x40026400 | AHB | 0x40020400 |
| DMA1 | | 0x40026000 | | 0x40020000 |
| FLASH | | 0x40023C00 | | 0x40022000 |
| CRM | | 0x40023800 | | 0x40021000 |
| SDIO1 | N/A | N/A | | 0x40018000 |
| GPIOF | AHB | 0x40021400 | APB2 | 0x40011C00 |
| GPIOE | | 0x40021000 | N/A | N/A |
| GPIOD | | 0x40020C00 | APB2 | 0x40011400 |
| GPIOC | | 0x40020800 | | 0x40011000 |
| GPIOB | | 0x40020400 | | 0x40010C00 |
| GPIOA | | 0x40020000 | | 0x40010800 |
| ACC | APB2 | 0x40017400 | N/A | N/A |
| TMR11 | | 0x40014800 | APB2 | 0x40015400 |
| TMR10 | | 0x40014400 | | 0x40015000 |
| TMR9 | | 0x40014000 | | 0x40014C00 |
| EXINT | | 0x40013C00 | | 0x40010400 |
| SCFG | | 0x40013800 | N/A | N/A |
| ADC | | 0x40012000 | APB2 | 0x40012400 |
| USART6 | | 0x40011400 | N/A | N/A |
| USART1 | | 0x40011000 | APB2 | 0x40013800 |
| IOMUX | N/A | N/A | | 0x40010000 |
| TMR1 | APB2 | 0x40010000 | | 0x40012C00 |
| USART8 | APB1 | 0x40007C00 | N/A | N/A |
| USART7 | | 0x40007800 | | |
| DAC | | 0x40007400 | | |
| CAN2 | | 0x40006800 | | |
| CAN1 | | 0x40006400 | | |
| I2C3 | | 0x40005C00 | | |
| SPI3 | | 0x40003C00 | | |
| CMP | N/A | N/A | APB1 | 0x40002400 |
| TMR14 | APB1 | 0x40002000 | N/A | N/A |
| TMR13 | | 0x40001C00 | | |
| TMR12 | | 0x40001800 | | |

| Peripheral | AT32F423 | | AT32F415 | |
|---|---|---|---|---|
| | Bus | Base address | Bus | Base address |
| TMR7 | | 0x40001400 | | |
| TMR6 | | 0x40001000 | | |
| TMR5 | N/A | N/A | APB1 | 0x40000C00 |

### 4.2.2 Interrupt vectors

- *Table 7* presents the interrupt vector differences in AT32F423 series versus AT32F415 series.

**Table 7. Interrupt vector differences**

| Position | AT32F423 | AT32F415 |
|---|---|---|
| 0 | WWDT | WWDT |
| 1 | PVM | PVM |
| 2 | TAMPER | TAMPER |
| 3 | ERTC_WKUP | ERTC |
| 4 | FLASH | FLASH |
| 5 | CRM | CRM |
| 6 | EXINT0 | EXINT0 |
| 7 | EXINT1 | EXINT1 |
| 8 | EXINT2 | EXINT2 |
| 9 | EXINT3 | EXINT3 |
| 10 | EXINT4 | EXINT4 |
| 11 | DMA1_CH1 | DMA1_CH1 |
| 12 | DMA1_CH2 | DMA1_CH2 |
| 13 | DMA1_CH3 | DMA1_CH3 |
| 14 | DMA1_CH4 | DMA1_CH4 |
| 15 | DMA1_CH5 | DMA1_CH5 |
| 16 | DMA1_CH6 | DMA1_CH6 |
| 17 | DMA1_CH7 | DMA1_CH7 |
| 18 | ADC1 | ADC1 |
| 19 | CAN1_TX | CAN1_TX |
| 20 | CAN1_RX0 | CAN1_RX0 |
| 21 | CAN1_RX1 | CAN1_RX1 |
| 22 | CAN1_SE | CAN1_SE |
| 23 | EXINT9_5 | EXINT9_5 |
| 24 | TMR1_BRK_TMR9 | TMR1_BRK_TMR9 |
| 25 | TMR1_OVF_TMR10 | TMR1_OVF_TMR10 |
| 26 | TMR1_TRG_HALL_TMR11 | TMR1_TRG_HALL_TMR11 |
| 27 | TMR1_CH | TMR1_CH |
| 28 | TMR2 | TMR2 |
| 29 | TMR3 | TMR3 |
| 30 | TMR4 | TMR4 |
| 31 | I2C1_EVT | I2C1_EVT |
| 32 | I2C1_ERR | I2C1_ERR |
| 33 | I2C2_EVT | I2C2_EVT |
| 34 | I2C2_ERR | I2C2_ERR |
| 35 | SPI1 | SPI1 |
| 36 | SPI2 | SPI2 |
| 37 | USART1 | USART1 |
| 38 | USART2 | USART2 |

| Position | AT32F423 | AT32F415 |
|---|---|---|
| 39 | USART3 | USART3 |
| 40 | EXINT15_10 | EXINT15_10 |
| 41 | ERTCAlarm | ERTCAlarm |
| 42 | OTGFS1_WKUP | OTGFS1_WKUP |
| 43 | TMR12 | Reserved |
| 44 | TMR13 | Reserved |
| 45 | TMR14 | Reserved |
| 46 | Reserved | Reserved |
| 47 | Reserved | Reserved |
| 48 | Reserved | Reserved |
| 49 | Reserved | SDIO1 |
| 50 | Reserved | TMR5 |
| 51 | SPI3 | Reserved |
| 52 | USART4 | UART4 |
| 53 | USART5 | UART5 |
| 54 | TMR6_DAC | Reserved |
| 55 | TMR7 | Reserved |
| 56 | DMA2_CH1 | DMA2_CH1 |
| 57 | DMA2_CH2 | DMA2_CH2 |
| 58 | DMA2_CH3 | DMA2_CH3 |
| 59 | DMA2_CH4 | DMA2_CH5_4 |
| 60 | DMA2_CH5 | Reserved |
| 61 | Reserved | Reserved |
| 62 | Reserved | Reserved |
| 63 | CAN2_TX | Reserved |
| 64 | CAN2_RX0 | Reserved |
| 65 | CAN2_RX1 | Reserved |
| 66 | CAN2_SE | Reserved |
| 67 | OTGFS1 | OTGFS1 |
| 68 | DMA2_CH6 | Reserved |
| 69 | DMA2_CH7 | Reserved |
| 70 | Reserved | CMP1 |
| 71 | USART6 | CMP2 |
| 72 | I2C3_EVT | Reserved |
| 73 | I2C3_ERR | Reserved |
| 74 | Reserved | Reserved |
| 75 | Reserved | DMA2_CH7_6 |
| 76 | Reserved | Reserved |
| 77 | Reserved | Reserved |
| 78 | Reserved | Reserved |
| 79 | Reserved | Reserved |
| 80 | Reserved | Reserved |
| 81 | FPU | Reserved |

| Position | AT32F423 | AT32F415 |
|---|---|---|
| 82 | USART7 | Reserved |
| 83 | USART8 | Reserved |
| 84 | Reserved | Reserved |
| 85 | Reserved | Reserved |
| 86 | Reserved | Reserved |
| 87 | Reserved | Reserved |
| 88 | Reserved | Reserved |
| 89 | Reserved | Reserved |
| 90 | Reserved | Reserved |
| 91 | Reserved | Reserved |
| 92 | Reserved | Reserved |
| 93 | Reserved | Reserved |
| 94 | DMAMUX | Reserved |
| 95 | Reserved | Reserved |
| 96 | Reserved | Reserved |
| 97 | Reserved | Reserved |
| 98 | Reserved | Reserved |
| 99 | Reserved | Reserved |
| 100 | Reserved | Reserved |
| 101 | Reserved | Reserved |
| 102 | Reserved | Reserved |
| 103 | ACC | Reserved |

### 4.2.3 ADC interface

- AT32F423 series embeds an enhanced ADC peripheral compared to AT32F415 series. *Table 8* presents the differences of ADC interface.

**Table 8. ADC interface differences**

| ADC | AT32F423 | | AT32F415 | |
|---|---|---|---|---|
| Channel | Up to 27 channels | | Up to 18 channels | |
| Resolution | 6/8/10/12-bit | | 12-bit | |
| Max sampling frequency | Up to 5.33 MSPS | | Up to 2 MSPS | |
| Oversampling | 2 to 256 times hardware oversampling | | Not support | |
| External trigger | Regular group<br>TMR1_TRGOUT<br>TMR1_CH4<br>TMR2_TRGOUT<br>TMR3_TRGOUT<br>TMR9_TRGOUT<br>TMR1_CH1<br>EXINT_Line11 | Preempted group<br>TMR1_CH2<br>TMR1_CH3<br>TMR2_CH4<br>TMR3_CH4<br>TMR9_CH1<br>TMR6_TRGOUT<br>EXINT_Line15 | Regular group<br>TMR1_CH1<br>TMR1_CH2<br>TMR1_CH3<br>TMR2_CH2<br>TMR3_TRGOUT<br>TMR4_CH4<br>EXINT_Line11 | Preempted group<br>TMR1_TRGOUT<br>TMR1_CH4<br>TMR2_TRGOUT<br>TMR2_CH1<br>TMR3_CH4<br>TMR4_TRGOUT<br>EXINT_Line15 |

| | | | | |
|---|---|---|---|---|
| | OCSWTRG | PCSWTRG | TMR1_TRGOUT<br>OCSWTRG<br>TMR1_TRGOUT | TMR1_CH4<br>PCSWTRG<br>TRM1_CH1 |
| Conversion stop | Conversion can be stopped during the sequence of conversion | | Not support | |
| Overflow detection | Support overflow detection (with flag bits and interrupts) | | Not support | |
| Data read | Support CPU read and DMA read<br>Support DMAMUX, flexible channel configuration, refer to DMA interface for details | | Support CPU read and DMA read<br>DMA supports fixed mapping and flexible mapping mode, refer to DMA interface for details | |

### 4.2.4 CAN interface

- AT32F423 CAN peripheral is the same as that of AT32F415, and they are software compatible. The only difference is that the AT32F423 features two CAN interfaces versus AT32F415.

### 4.2.5 CRM interface

- AT32F423 CRM (clock and reset management) interface has big differences with that of AT32F415. They are software-incompatible. The main differences are as follows:

  1. **PLL configuration:**

     **AT32F423:** its PLL uses flexible mode, the frequency multiplication format is

     PLLCLK = (PLL reference clock * PLL_NS) / (PLL_MS * PLL_FR);

     **AT32F415:** its PLL supports both flexible mode and common mode.

     The frequency multiplication format in flexible mode is PLLCLK = (PLL reference clock * PLL_NS) / (PLL_MS * PLL_FR), while the format in common mode is PLLCLK = PLL reference clock * PLL_MULT.

  2. Peripheral clock low-power mode: peripheral clock can be disabled when entering Sleep mode.

     AT32F423: each of its peripherals can be configured with this feature individually;

     AT32F415: only its SRAM and Flash can be configured with this feature.

  3. For AT32F423, when HEXT or HICK is directly used as system clock, it is also possible to first divide this clock and then provide it to system clock

  4. For AT32F423, HICK 48 MHz can be directly provided to USB, but not for AT32F415.

- References are made to the following documents:

  《AN0158_AT32F423_CRM_Start_Guide》

  《AN0117_AT32F415_CRM_Start_Guide》

### 4.2.6 DMA interface

- AT32F415 DMA supports fixed mapping and flexible mapping modes;

  AT32F423 DMA supports DMAMUX with more functions (flexible mapping, DMA request synchronization, DMA request generation)

- References are made to the following documents:

  《AN0160_AT32F423_DMA_Application_Note》

### 4.2.7 Flash interface

- *Table 9* presents the differences between AT32F423 series and AT32F415 in terms of Boot memory and User System Data area.

**Table 9. Flash memory address differences**

| Memory | AT32F423 | AT32F415 |
|---|---|---|
| Boot memory | 0x1FFFA400-0x1FFFF3FF | 0x1FFFAC00-0x1FFFF3FF |
| User System Data area | 0x1FFFF800-0x1FFFF9FF | 0x1FFFF800-0x1FFFFBFF |

- If Bootloader is not needed for users, the boot memory can be one-time configurable to general user program and data area.

### 4.2.8 ERTC interface

- The differences related to ERTC peripheral in AT32F423 versus AT32F415 include:
  1. AT32F423 offers tamper detection 2 feature, but not for AT32F415
  2. AT32F423 has no VBAT pin and thus cannot be supplied via this pin;

     AT32F415 has VBAT pin and thus can be supplied via this pin

### 4.2.9 EXINT interrupt source selection

- In AT32F423 series, external interrupt configuration mode presents some differences vs. AT32F415 series:

  AT32F415 uses IOMUX_EXINTCx register to configure external interrupts;

  AT32F423 uses SCFG_EXINTCx register to configure external interrupts.

  Actually, only the mapping addresses of the EXINTCx registers have changed, but the logics of EXINTx configuration are the same.

### 4.2.10 GPIO interface

- The differences related to GPIO peripheral in the AT32F423 series versus AT32F415 series are as follows:

  **AT32F423:**

  The GPIOs are configured through three registers, GPIOx_CFGR register (configure IO operating mode), GPIOx_OMODE register (configure output mode) and GPIOx_PULL register (configure IO pull-up/pull-down). The IO pull-up/pull-down configurations apply to the general-purpose input/output mode and alternate function mode.

  A few FTf GPIO is capable of outputting 20 mA low level.

  **AT32F415:**

  AT32F415 series GPIOs are configured through two registers, GPIOx_CFGLR and GPIOx_CFGHR. These registers can be used to configure IO operating mode, output mode and IO pull-up/pull-down mode. But its IO pull-up/pull-down configurations only apply to input mode.

- References are made to the following documents:

  《AN0119_AT32F413_415_GPIO_Application_Note》

  《AN0162_AT32F423_GPIO_Application_Note》

### 4.2.11 I²C interface

- In AT32F423 series, the I2C interface presents big differences vs. AT32F415 series. They are software-incompatible.

  The control logic of AT32F423 I2C is made easier than that of AT32F415. Also, the AT32F423 has an additional Fast Mode Plus (up to 1 MHz) and low-power wakeup feature compared with AT32F415 I2C.

- References are made to the following documents:

  《AN0159_AT32F423_I2C_Application_Note》

### 4.2.12 IOMUX

- The differences related to IOMUX peripheral in the AT32F423 series versus AT32F415 series are described as follows:

  **AT32F423:**

  For AT32F423 series, for any peripherals to use alternate functions, the I/O must be configured as alternate functions.

  Pin multiplexing and mapping are configured through the GPIOx_MUXL and GPIOx_MUXH registers.

  **AT32F415:**

  Whether or not the I/O should be used as alternate function depends on the peripheral mode used. For example, USART Tx pin should be configured as alternate function push-pull, while the USART Rx should be input floating or input pull-up.

  To optimize the number of peripheral I/O functions on different packages, it is possible to remap some alternate functions to other pins. The IOMUX_REMAPx register is used to configure the alternate functions of the peripheral pins.

- References are made to the following documents:

  《AN0119_AT32F413_415_GPIO_Application_Note》

  《AN0162_AT32F423_GPIO_Application_Note》

### 4.2.13 PWC interface

**Table 10. PWC interface differences**

| PWR | AT32F423 | AT32F415 |
|---|---|---|
| Standby mode wakeup pin | 4 x WKUP pins | 1 x WKUP pin |
| Internal voltage regulator | Support extra low-power mode of the internal voltage regulator in Deepsleep mode.<br>The low-power consumption level of internal voltage regulator is settable. | Not support |

- *Table 10* presents the differences between the PWR interface of the AT32F423 series and AT32F415 series.
  Compared to AT32F415, the AT32F423 series adds three more Standby-mode WKUP pins in order to adapt to diverse application scenarios.
- AT32F423 series supports extra low-power consumption mode of internal voltage regulator after Deepsleep mode is entered. By doing so, it is possible to save more power in Deepsleep mode.
- In AT32F423 series, the internal voltage regulator is configurable in order to further optimize the tradeoff between MCU performance and power consumption.
- References are made to the following documents:

  《AN0163_AT32F423_PWC_Application_Note》

### 4.2.14 SPI interface

- AT32F423 series offers newly-added features on the back of AT32F415 series:
  1. Support divided-by-3 setting using the MDIV3EN bit in SPI_CTRL2 register
  2. TI mode, enabled through the TIEN control bit in SPI_CTRL2 register.
  3. I2S full-duplex mode, enabled through the I2S_FD bit in the SCFG_CFG2 register.

### 4.2.15 Security library interface

- The security library of the AT32F423 series is optimized compared to the AT32F415, with slight differences.
- References are made to the following documents:

  《AN0164_AT32F423_Security_Library_Application_Note》

### 4.2.16 TMR interface

- In AT32F423 series, the TMRx_RPR register (repetition period register) of the advanced timer TMR1 is extended to 16-bit
- In AT32F423 series, TMR9/10/11/12/13/14 boast repetition period register (TMRx_RPR) that is extended to 16-bit
- In AT32F423 series, TMR9/10/11/12/13/14 support DMA-related features, which are configured through the TMRx_DMACTRL and TMRx_DMADT registers
- In AT32F423 series, TMR9/10/11/12/13/14 support break-related features, which are configured through the OEN/ AOEN/ BRKV/ BRKEN bits in TMRx_ BRK register
- In AT32F423 series, TMR1/9/10/11/12/13/14 support break input filtering feature, which is configured through the BKF bit in TMRx_ BRK register

### 4.2.17 WDT interface

- In AT32F423 series, WDT peripheral supports windowed WDT feature, meaning that it can stop counting in Deepsleep and Standby modes. Except for this point, other WDT functions are the same as those of AT32F415, and both series are software-compatible. AT32F423 is downward compatible with AT32F415.

### 4.2.18 USART interface

- In addition to the original features of AT32F415, the AT32F423 offers additional features below:
  1. Serial interface low-power wakeup feature
  2. TX/RX SWAP feature
  3. RS485 communication mode
  4. 7-bit data length mode

## 4.3 Peripheral enhancement

### 4.3.1 AT32F423 additional WKUP pins

- Apart from retaining the original WKUP pins (WKUP1-PA0) of AT32F415, the AT32F423 series offers three more Standby-mode WKUP pins.

  WKUP pin 2——PC13

  WKUP pin 6——PB5

  WKUP pin 7——PB15

  These three WKUP pins have their respective enable bits (refer to the corresponding datasheet and technical manual for more information). When enabled, the wake-up events on the corresponding pin can wake up Standby mode. It is also possible to enable one or more wake-ups pins to wake up Standby mode according to the actual requirements.

### 4.3.2 AT32F423 infrared transmitter

- This infrared transmitter is based on the internal connection between TMR110 and USART1, or USART2 and TMR11.

  The TMR11 is used to provide carrier frequency, while the TMR10, USART1 or USART2 provides the main signals to be sent.

  The infrared output signal is available on PB9 or PA13.

### 4.3.3 AT32F423 TMR 16-bit RPR register

- The RPR (repetition period) register of TMR is extended from 8-bit to 16-bit. In single-pulse mode, it is possible to configure RPR register to achieve multi-pulse function, sending up to 65536 pulses at one time.

### 4.3.4 AT32F423 HICK auto clock calibration module

- HICK auto clock calibration (ACC) module uses the SOF signal (1 ms period) coming from the USB module as a reference signal to perform HICK clock sampling and calibration.

  This feature is mainly used to provide the USB device with 48 MHz±0.25% accuracy clock. Crystal-less mode is supported.

### 4.3.5 AT32F423 OTGFS device endpoints and host channels

- In device mode, OTGFS supports one bidirectional control endpoint, seven IN endpoints and seven OUT endpoints.
- In host mode, OTGFS supports 16 host channels.

### 4.3.6 AT32F423 XMC peripheral

- Support address lines/data lines to be used as storage memory, such as multiplexed PSRAM
- Support LCD parallel interface, such as 8080 mode

### 4.3.7 AT32F423 DAC peripheral

- DAC peripheral is embedded in the AT32F423 series. This DAC has DMA underflow detection function, with the DMA underflow flag being stored in the DAC_STS register. Besides, the DAC comes with DAC underflow error interrupt enable bit and interrupt vector.

### 4.3.8 AT32F423 full-duplexed I2S function

- AT32F423 offers I2S full-duplex function compared to AT32F415. It is possible to use any two of I2S1/I2S2/I2S3 to achieve full-duplexed I2S function according to actual requirements.

  After I2S full-duplexed mode is configured, the IO remap relationship on the host side (I2S1/I2S2) remains unchanged. The SCK and WS of I2S2/I2S3 (as device) are connected internally to the SCK and WS of the host. The SD line on the device side is remapped to I2Sext_SD, and the previous IO remap relationship on the device side is deactivated, with the corresponding IOs being released.

### 4.3.9 AT32F423 SPI TI mode

- AT32F423 supports SPI TI mode vs. AT32F415.

  The SPI interface of AT32F423 supports TI protocols. After TI mode is enabled, SPI interface communications follow strictly with the TI protocols, including generating communication clocks and CS signals that are compatible with polarity phase characteristics.

### 4.3.10 AT32F423 GPIO toggle function

- In AT32F423 series, the GPIO bits can be toggled by writing “1” to a certain bit in the GPIO TOGR register. By doing so, the corresponding bits in the ODT (output data) register will be reversed to their original values.

# 5 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 2023.01.13 | 2.0.0 | Initial release |

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