MG0026
Migration Guide

Migrating from AT32F415 to AT32A423

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing AT32F415 series to AT32A423 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from AT32F415 series to AT32A423 series, users have to analyze the hardware and software migration.

Applicable products:

Part number	AT32A423xx

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1 Similarities and differences between AT32A423 and AT32F415

AT32A423 series microcontrollers are basically compatible with the AT32F415 series, and provide many enhanced features, some of which are different from AT32F415. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, the alternate functions of pins are defined.
- Compiler tools: identical, for example, Keil, IAR, AT32 IDE.

1.2 Overview of differences

Table 1. Differences between AT32A423 and AT32F415

	AT32A423	AT32F415
System clock	Max. frequency 150 MHz, APB1 120 MHz, APB2 150 MHz	Max. frequency 150 MHz, APB1 75 MHz, APB2 75 MHz
FPU	Support	NA
Wake up from Deepsleep (LDO in low-power mode)	500us	360us
Wake up from Standby mode	800us	600us
SRAM size	32/48 KB	32 KB
Bootloader	20 KB, support USART3	18 KB
16-bit timer	8	6
32-bit time	1	2
Basic timer	2	-
ACC	Support	-
CMP	-	2
ADC	5.33 MSPS, 27 channels	2 MSPS, 16 channels
DAC	2 channels	--
DMA	Support DMAMUX	Not support DMAMUX
CAN	2	1
SPI/I2S	3	2
SDIO	-	1
USART	8	5
XMC	Support	-
OTG device endpoint	8 IN, 8 OUT (include endpoint 0)	4 IN, 4 OUT (include endpoint 0)
Number of OTG master channels	16	8
Operating supply	2.4 V~3.6 V	2.6 V~3.6 V
V_{BAT} supply	-	Support
ESD	HBM: 4 KV, CDM: 1 KV	HBM: 5 KV, CDM: 1 KV
Typical current in Run mode	20.4mA@72Mhz with all peripherals enabled	24.6mA@72Mhz with all peripherals enabled

	AT32A423	AT32F415
Typical current in Sleep mode	16.5mA@72Mhz with all peripherals enabled	19.7mA@72Mhz with all peripherals enabled
Typical current in Deepsleep mode (LDO in low-power mode)	143uA	680uA
Typical current in Standby mode	5.4uA	6.6uA
Packages	Support LQFP100 and add QFN36	Support LQFP64

2 Hardware migration

AT32A423 series is pin-to-pin compatible with AT32F415 series for the same packages. As they differ in the GPIO peripheral, it is necessary to refer to the corresponding Datasheet for more information on the peripheral functions of each pin.

Table 2. Peripheral compatibility analysis

AT32A423					AT32F415				
LQFP64	LQFP48	QFN48	QFN32	Pin name	LQFP64	LQFP48	QFN48	QFN32	Pin name
5	5	5	2	PF0	5	5	5	2	PD0
6	6	6	3	PF1	6	6	6	3	PD1
18	-	-	-	Vss	18	-	-	-	PF4
19	-	-	-	Vdd	19	-	-	-	PF5
31	23	23	-	PF8	31	23	23	-	Vss
48	36	36	-	Vdd	48	36	36	-	PF7

3 Boot mode compatibility

In most cases, AT32A423 and AT32F415 series load a Boot mode on a system reset. However, for AT32A423 series, if embedded SRAM Boot mode is selected, the BOOT status is then locked. In this case, it is impossible to load a new Boot mode on a system reset unless a power-on reset occurs.

AT32F415 series observes the configuration of the Boot mode selection in Table 3. The BOOT0 and BOOT1 state correspond to the level on the BOOT0 and BOOT1 pins, respectively.

Table 3. AT32F415 boot mode

Boot mode selection		Boot mode	Description
BOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	Boot memory	Boot memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

AT32A423 series observes the configuration of the Boot mode selection in Table 4. BOOT0 state corresponds to the level on the BOOT0 pin, while the nBOOT1 corresponds to the nBOOT1 bit value of the system configuration byte (SSB) within the User System Data (USD).

Table 4. AT32A423 boot mode

Boot mode selection		Boot mode	Description
nBOOT1	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
1	1	Boot memory	Boot memory is selected as boot space
0	1	Embedded SRAM	Embedded SRAM is selected as boot space

4 Software migration

4.1 Peripheral comparison

AT32A423 series is mostly compatible with AT32F415 series in terms of peripherals, except for a few function enhancements or new designs. Thus it is necessary to modify these peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 5. Peripheral compatibility analysis

Peripheral	AT32A423	AT32F415	Compatibility	
			Pinout	Firmware driver
PWC	Y	Y	NA	Partial compatibility
CRM	Y	Y	Identical	Partial compatibility
CMP	NA	Y	NA	Incompatible
FLASH	Y	Y	NA	Partial compatibility
GPIO	Y	Y	Identical	Incompatible
IOMUX	NA	Y	NA	Incompatible
SCFG	Y	NA	NA	Incompatible
EXINT	Y	Y	Identical	Partial compatibility
DMA	Y	Y	NA	Partial compatibility
CRC	Y	Y	NA	Full compatibility
I2C	Y	Y	Identical	Incompatible
USART	Y	Y	Identical	Partial compatibility
SPI	Y	Y	Identical	Partial compatibility
TMR	Y	Y	Identical	Partial compatibility
WWDT	Y	Y	NA	Full compatibility
WDT	Y	Y	NA	Full compatibility
RTC	Y	Y	Identical	Partial compatibility
ADC	Y	Y	Identical	Incompatible
DAC	Y	NA	NA	Incompatible
CAN	Y	Y	Identical	Full compatibility
OTGFS	Y	Y	Identical	Partial compatibility
ACC	Y	NA	NA	Incompatible
IRTMR	Y	NA	NA	Incompatible
SDIO	NA	Y	NA	Incompatible
DEBUG	Y	Y	NA	Incompatible
XMC	Y	NA	NA	Incompatible

4.2 Functional differences

This section describes the peripheral differences in the AT32A423 series versus AT32F415 series.

The peripheral behavior of the AT32A423 series is detailed in the subsections below.

4.2.1 Memory mapping

- Table 6 presents the differences related to address mapping and bus distribution in AT32A423 versus AT32F415.

Table 6. Memory map differences

Peripheral	AT32A423		AT32F415	
	Bus	Base address	Bus	Base address
XMC	AHB	0xA0000000	N/A	N/A
DMA2		0x40026400	AHB	0x40020400
DMA1		0x40026000		0x40020000
FLASH		0x40023C00		0x40022000
CRM		0x40023800		0x40021000
SDIO1	N/A	N/A		0x40018000
GPIOF	AHB	0x40021400	APB2	0x40011C00
GPIOE		0x40021000	N/A	N/A
GPIOD		0x40020C00	APB2	0x40011400
GPIOC		0x40020800		0x40011000
GPIOB		0x40020400		0x40010C00
GPIOA		0x40020000		0x40010800
ACC	APB2	0x40017400	N/A	N/A
TMR11		0x40014800	APB2	0x40015400
TMR10		0x40014400		0x40015000
TMR9		0x40014000		0x40014C00
EXINT		0x40013C00		0x40010400
SCFG		0x40013800	N/A	N/A
ADC		0x40012000	APB2	0x40012400
USART6		0x40011400	N/A	N/A
USART1		0x40011000	APB2	0x40013800
IOMUX	N/A	N/A		0x40010000
TMR1	APB2	0x40010000		0x40012C00
USART8	APB1	0x40007C00	N/A	N/A
USART7		0x40007800		
DAC		0x40007400		
CAN2		0x40006800		
CAN1		0x40006400		
I2C3		0x40005C00		
SPI3		0x40003C00		
CMP	N/A	N/A	APB1	0x40002400
TMR14	APB1	0x40002000	N/A	N/A
TMR13		0x40001C00		
TMR12		0x40001800		
TMR7		0x40001400		
TMR6		0x40001000		
TMR5	N/A	N/A	APB1	0x40000C00

4.2.2 Interrupt vectors

- Table 7 presents the interrupt vector differences in AT32A423 series versus AT32F415 series.

Table 7. Interrupt vector differences

Position	AT32A423	AT32F415
0	WWDT	WWDT
1	PVM	PVM
2	TAMPER	TAMPER
3	ERTC_WKUP	ERTC
4	FLASH	FLASH
5	CRM	CRM
6	EXINT0	EXINT0
7	EXINT1	EXINT1
8	EXINT2	EXINT2
9	EXINT3	EXINT3
10	EXINT4	EXINT4
11	DMA1_CH1	DMA1_CH1
12	DMA1_CH2	DMA1_CH2
13	DMA1_CH3	DMA1_CH3
14	DMA1_CH4	DMA1_CH4
15	DMA1_CH5	DMA1_CH5
16	DMA1_CH6	DMA1_CH6
17	DMA1_CH7	DMA1_CH7
18	ADC1	ADC1
19	CAN1_TX	CAN1_TX
20	CAN1_RX0	CAN1_RX0
21	CAN1_RX1	CAN1_RX1
22	CAN1_SE	CAN1_SE
23	EXINT9_5	EXINT9_5
24	TMR1_BRK_TMR9	TMR1_BRK_TMR9
25	TMR1_OVF_TMR10	TMR1_OVF_TMR10
26	TMR1_TRG_HALL_TMR11	TMR1_TRG_HALL_TMR11
27	TMR1_CH	TMR1_CH
28	TMR2	TMR2
29	TMR3	TMR3
30	TMR4	TMR4
31	I2C1_EVT	I2C1_EVT
32	I2C1_ERR	I2C1_ERR
33	I2C2_EVT	I2C2_EVT
34	I2C2_ERR	I2C2_ERR
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	USART3	USART3

Position	AT32A423	AT32F415
40	EXINT15_10	EXINT15_10
41	ERTCAlarm	ERTCAlarm
42	OTGFS1_WKUP	OTGFS1_WKUP
43	TMR12	Reserved
44	TMR13	Reserved
45	TMR14	Reserved
46	Reserved	Reserved
47	Reserved	Reserved
48	Reserved	Reserved
49	Reserved	SDIO1
50	Reserved	TMR5
51	SPI3	Reserved
52	USART4	UART4
53	USART5	UART5
54	TMR6_DAC	Reserved
55	TMR7	Reserved
56	DMA2_CH1	DMA2_CH1
57	DMA2_CH2	DMA2_CH2
58	DMA2_CH3	DMA2_CH3
59	DMA2_CH4	DMA2_CH5_4
60	DMA2_CH5	Reserved
61	Reserved	Reserved
62	Reserved	Reserved
63	CAN2_TX	Reserved
64	CAN2_RX0	Reserved
65	CAN2_RX1	Reserved
66	CAN2_SE	Reserved
67	OTGFS1	OTGFS1
68	DMA2_CH6	Reserved
69	DMA2_CH7	Reserved
70	Reserved	CMP1
71	USART6	CMP2
72	I2C3_EVT	Reserved
73	I2C3_ERR	Reserved
74	Reserved	Reserved
75	Reserved	DMA2_CH7_6
76	Reserved	Reserved
77	Reserved	Reserved
78	Reserved	Reserved
79	Reserved	Reserved
80	Reserved	Reserved
81	FPU	Reserved
82	USART7	Reserved
83	USART8	Reserved

Position	AT32A423	AT32F415
84	Reserved	Reserved
85	Reserved	Reserved
86	Reserved	Reserved
87	Reserved	Reserved
88	Reserved	Reserved
89	Reserved	Reserved
90	Reserved	Reserved
91	Reserved	Reserved
92	Reserved	Reserved
93	Reserved	Reserved
94	DMAMUX	Reserved
95	Reserved	Reserved
96	Reserved	Reserved
97	Reserved	Reserved
98	Reserved	Reserved
99	Reserved	Reserved
100	Reserved	Reserved
101	Reserved	Reserved
102	Reserved	Reserved
103	ACC	Reserved

4.2.3 ADC interface

- AT32A423 series embeds an enhanced ADC peripheral compared to AT32F415 series. Table 8 presents the differences of ADC interface.
- References

  AN0115_AT32F415_ADC_Application_Note

  AN0203_AT32A423_ADC_Application_Note

Table 8. ADC interface differences

ADC	AT32A423		AT32F415	
Channel	Up to 27 channels		Up to 18 channels	
Resolution	6/8/10/12-bit configurable		Fixed 12-bit	
Sampling	Up to 5.33 MSPS		Up to 2 MSPS	
Oversampling	2 to 256 times hardware oversampling		Not support	
External trigger	Regular group TMR1_TRGOUT TMR1_CH4 TMR2_TRGOUT TMR3_TRGOUT TMR9_TRGOUT TMR1_CH1 EXINT_Line11 OCSWTRG	Preempted group TMR1_CH2 TMR1_CH3 TMR2_CH4 TMR3_CH4 TMR9_CH1 TMR6_TRGOUT EXINT_Line15 PCSWTRG	Regular group TMR1_CH1 TMR1_CH2 TMR1_CH3 TMR2_CH2 TMR3_TRGOUT TMR4_CH4 EXINT_Line11 TMR1_TRGOUT	Preempted group TMR1_TRGOUT TMR1_CH4 TMR2_TRGOUT TMR2_CH1 TMR3_CH4 TMR4_TRGOUT EXINT_Line15 TMR1_CH4

ADC	AT32A423		AT32F415	
			OCSWTRG TMR1_TRGOUT	PCSWTRG TRM1_CH1
End of conversion	Support end of conversion during ADC sequence conversion		Not support	
Overflow detection	Support overflow detection, including the corresponding flags and interrupts		Not support	
Data access	Support data access through CPU and DMA Support DMAMUX for more flexible channel configuration (see DMA interface for details)		Support data access through CPU and DMA Support fixed and flexible mapping (see DMA interface for details)	

4.2.4 CAN interface

- AT32A423 series is compatible with AT32F415 in terms of CAN, except that AT32A423 series has one more CAN interface.

4.2.5 CRM interface

- There are some differences between the CRM interfaces between AT32A423 and AT32F415. They are incompatible in software.
  1. PLL configuration: AT32A423 series supports flexible PLL configuration, formula: PLLCLK = (PLL reference clock * PLL_NS) / (PLL_MS * PLL_FR); while AT32F415 series supports flexible and regular configurations, formula (flexible): PLLCLK = (PLL reference clock * PLL_NS) / (PLL_MS * PLL_FR), formula (regular): PLLCLK = PLL reference clock * PLL_MULT.
  2. Peripheral clock low-power mode: Peripheral clock can be disabled when entering Sleep mode to reduce power consumption. For AT32A423 series, each peripheral can be configured independently; for AT32F415 series, only SRAM and FLASH can be configured.
  3. AT32A423 supports frequency division when HEXT or HICK is used as system clock directly.
  4. AT32A423 supports HICK 48MHz to be used as USB clock directly, while AT32F415 does not support.
- References

  AN0204_AT32A423_CRM_Start_Guide

  AN0117_AT32F415_CRM_Start_Guide

4.2.6 DMA interface

- AT32F415 series supports DMA flexible and fixed mapping, while AT32A423 series supports DMAMUX (flexible mapping, DMA request synchronization, and DMA request generation) with more functions.
- References

  AN0205_AT32A423_DMA_Application_Note

4.2.7 Flash interface

- Table 9 presents the differences between AT32A423 and AT32F415 in terms of boot memory and User System Data area.

Table 9. Flash memory address differences

Memory	AT32A423	AT32F415
Boot memory	0x1FFFA400-0x1FFFF3FF	0x1FFFAC00-0x1FFFF3FF
User System Data area	0x1FFFF800-0x1FFFF9FF	0x1FFFF800-0x1FFFFBFF

- The boot memory can be used as a bootloader or as a general instruction/data memory (one-time configured).

4.2.8 ERTC interface

- There are some differences between AT32A423 and AT32F415 in terms of ERTC, including
  1. AT32A423 series ERTC has two tamper detection modes, while AT32F415 series ERTC has only one tamper detection mode.
  2. AT32A423 series has no V_{BAT} pin and does not support V_{BAT} supply, while AT32F415 series has a V_{BAT} pin for power supply.

4.2.9 EXINT interrupt source selection

- There are some differences between the external interrupt configuration mode of the AT32A423 series and AT32F415 series. The AT32F415 series uses the IOMUX_EXINTCx register to configure external interrupts, while the AT32A423 series uses the SCFG_EXINTCx register. In this way, only the mapping address of the EXINTCx register has changed, without any change to the meaning of EXINTx configuration.

4.2.10 GPIO

- The differences related to GPIO peripheral in the AT32A423 series versus AT32F415 series are described as follows.

  AT32A423:

  AT32A423 series GPIOs are configured through the GPIOx_CFGR register (configure IO operating mode), GPIOx_OMODE register (configure output mode) and GPIOx_PULL register (configure IO pull-up/pull-down). The IO pull-up/pull-down configurations apply to the general-purpose input/output mode and multiplexed function mode.

  Some FTf GPIOs have 20 mA low output capability.

  AT32F415:

  AT32F415 series GPIOs are configured through the GPIOx_CFGLR and GPIOx_CFGHR registers. These registers can be used to configure IO operating mode, output mode and IO pull-up/pull-down mode. The IO pull-up/pull-down configurations apply to the input mode.

- References

  AN0119_AT32F413_415_GPIO_Application_Note

  AN0206_AT32A423_GPIO_Application_Note

4.2.11 I²C interface

- There are big differences between the I²C interfaces of AT32A423 versus AT32F415. They are incompatible in software.

  Compared with AT32F415, the AT32A423 series I²C has a simpler control logic and supports the fast mode plus (up to 1 MHz) and low-power wakeup functions.

- References

  AN0207_AT32A423_I2C_Application_Note

4.2.12 IOMUX

- The differences related to IOMUX of the AT32A423 series versus AT32F415 series are described as follows.

  AT32A423:

  For AT32A423 series, it is required that the I/O pin is configured as alternate function for peripherals to use I/O functions properly.

  Pin multiplexing and mapping are configured through the GPIOx_MUXL and GPIOx_MUXH registers.

  AT32F415:

  The I/O multiplexed function configuration depends on the peripheral mode used. For example, the USART_Tx pin should be configured as multiplexed push-pull, while the USART_Rx should be configured as floating input or pull-up input.

  To optimize the number of peripheral I/O functions on different packages, it is possible to remap some alternate functions to other pins. The IOMUX_REMAPx register is used to configure the alternate functions of the peripheral pins.

- References

  AN0119_AT32F413_415_GPIO_Application_Note

  AN0206_AT32A423_GPIO_Application_Note

4.2.13 PWC interface

Table 10. PWC interface differences

PWR	AT32A423	AT32F415
Standby mode wakeup pin	4 x WKUP pins	1 x WKUP pin
Internal voltage regulator (LDO)	Support extra low-power mode of LDO in Deepsleep mode The LDO power consumption level is configurable.	Not support

- Table 10 presents the differences between the PWC interface of the AT32A423 series and AT32F415 series. The AT32A423 series adds more WKUP pins from Standby mode in order to adapt to more application scenarios, compared to AT32F415.
- AT32A423 series allows to enable extra low-power mode of the LDO in Deepsleep mode. This feature helps further reduce power consumption when Deepsleep mode is enabled.
- AT32A423 series support LDO voltage regulating function to achieve balance between MCU performance and power consumption.

- References

  AN0208_AT32A423_PWC_Application_Note

4.2.14 SPI interface

- AT32A423 series has additional features compared to AT32F415 series:
  1. Clock prescaler selection: The master clock frequency divided by 3 is enabled by setting the MDIV3EN bit in the SPI_CTRL2 register.
  2. TI mode: This mode is enabled through the TIEN bit in the SPI_CTRL2 register.
  3. I^2S full-duplex mode: This mode is enabled through the I2S_FD bit in the SCFG_CFG2 register.

4.2.15 Security library (sLib) interface

- AT32A423 series optimizes security library (sLib) design compared to AT32F415 series.
- References

  AN0209_AT32A423_Security_Library_Application_Note

4.2.16 TMR interface

- In AT32A423, the repetition register (TMRx_RPR) of TMR1 (advanced timer) is expanded to be 16-bit register.
- In AT32A423, the repetition register (TMRx_RPR) is added for TMR9/10/11/12/13/14 timers, and is expanded to be 16-bit register.
- In AT32A423, TMR9/10/11/12/13/14 support DMA related functions, which can be configured through the TMRx_DMACTRL and TMRx_DMADT registers.
- In TMR peripheral, AT32A423 supports break related functions for TMR9/10/11/12/13/14 timers. This can be configured through the OEN/ AOEN/ BRKV/ BRKEN bit in the TMRx_BRK register.
- In TMR peripheral, AT32A423 supports break input filtering feature for TMR1/9/10/11/12/13/14 timers. This can be configured through the BKF bit in the TMRx_ BRK register.

4.2.17 WDT interface

- AT32A423 series adds window feature for WDT peripheral, and supports stopping counting in Deepsleep and Standby modes, with other functions being the same as those of AT32F415 series and software compatible. The AT32A423 series is downward compatible with AT32F415 series.

4.2.18 USART interface

- The AT32A423 series embeds an USART peripheral, which inherits USART feature of AT32F415 series and further extends functions including:
  1. Low-power mode wakeup pin
  2. Support TX/RX SWAP function
  3. Programmable communication mode: RS485
  4. Programmable data word length: 7 bits

4.3 Peripheral enhancement

4.3.1 AT32A423 additional WKUP pins

- Apart from retaining the original WKUP pins (WKUP1-PA0) used in AT32F415, the AT32A423 series provides additional three WKUP pins from Standby mode.

  WKUP pin 2——PC13

  WKUP pin 6——PB5

  WKUP pin 7——PB15

  These three WKUP pins have their respective enable bits (refer to the corresponding datasheet and technical manual for more information). When enabled, the wakeup event on the corresponding pin can wake up from Standby mode. It is possible to enable one or more wakeups pins to wake up from Standby mode according to the actual application requirements.

4.3.2 AT32A423 infrared transmitter

- The infrared transmitter is based on the internal connection between TMR10 and USART1, orUSART2 and TMR11. The TMR11 is used to provide carrier frequency, while the TMR10, USART1 or USART2 provides the main signals to be sent. The infrared output signal is available on PB9 or PA13.

4.3.3 AT32A423 TMR 16-bit RPR register

- The RPR (repetition period) register of the TMR is improved from 8-bit to 16-bit. In single-pulse mode, it is possible to configure RPP register to achieve multi-pulse function, which can send up to 65536 pulses at once.

4.3.4 AT32A423 HICK auto clock calibration module

- HICK auto clock calibration (ACC) uses the SOF signal (1 ms period) coming from the USB module as a reference signal to perform HICK clock sampling and calibration. This feature is mainly used to provide the USB device with 48 MHz ± 0.25% accuracy clock, supporting crystal-less.

4.3.5 AT32A423 OTGFS device endpoint and master channel

- In device mode, OTGFS supports one bidirectional control endpoint, seven IN endpoints and seven OUT endpoints.
- In master mode, OTGFS supports 16 master channels.

4.3.6 AT32A423 XMC peripheral

- Multiplexed address/data bus, such as multiplexed PSRAM
- XMC as LCD parallel interface, 8080 mode

4.3.7 AT32A423 DAC peripheral

- AT32A423 series has DAC peripheral and supports DMA underflow detection. It uses the DAC_STS register to store DMA underflow flag. In addition, it has the corresponding DAC underflow error interrupt enable bit and interrupt vector.

4.3.8 AT32A423 I²S full-duplex mode

- AT32A423 supports I²S full-duplex mode. Any two of I²S1/I²S2/I²S3 can be combined to achieve I²S full-duplex feature. In I²S full-duplex mode, the IO remap remains unchanged in the I²S full-duplex master side (I²S1/I²S2), while the SCK and WS in the I²S full-duplex slave side (I²S2/I²S3) are internally connected to the SCK and WS of the master side, SD line (slave side) is remapped on I2Sext_SD, and its original IO remap becomes invalid, with the corresponding IOs being released.

4.3.9 AT32A423 SPI TI mode

- The AT32A423 series SPI interface supports TI mode. In TI mode, the SPI interface performs communication in accordance with TI protocol, including generating a communication clock and a CS signal conforming to polarity and phase characteristics.

4.3.10 AT32A423 GPIO port bit toggle

- AT32A423 support GPIO port bit toggle. Writing “1” to the corresponding bit in the GPIO port bit toggle register (GPIOx_TOGR) will toggle the corresponding bit of the GPIO output data register (GPIOx_ODT).

5 Revision history

Table 11. Document revision history

Date	Version	Revision note
2024.03.06	2.0.0	Initial release.

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