MG0016
Migration Guide

Migrating from SXX32F030 to AT32F421

Introduction

This migration guide is written to help users with the analysis of the steps required to migrate from an existing SXX32F030 series to AT32F421 series. It brings together the most important information and lists the vital aspects that need to be taken into account.

To move an application from SXX32F030 series to AT32F421 series, users have to analyze the hardware and software migration.

Applicable products:

Part numbers	AT32F421xx

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1 Similarities and differences between AT32F421 and SXX32F030

AT32F421 series microcontrollers are mostly compatible with the SXX32F030 series, and provide many enhanced features, some of which are different from SXX32F030. The differences between them are detailed in this document.

1.1 Overview of similarities

- Pin definition: Pin definitions are identical for the same packages. For extended peripherals, the alternate functions of pins are defined.
- Compiler tools: identical, for example, Keil, IAR.

1.2 Overview of differences

Table 1. Differences between AT32F421 and SXX32F030

	AT32F421	SXX32F030
Core	Cortex-M4, and supports DSP instructions	Cortex-M0
System clock	Max frequency: 120 MHz, AHB/APB 120 MHz	Max frequency: 48 MHz, AHB/APB 48 MHz
Wake up from low-power mode (Voltage regulator is in low power mode)	450 µs	Max 9 µs
Wake up from Standby mode	1250 µs	60.4 µs
Flash size	64 KB	256 KB
SRAM size	16 KB	32 KB
Boot Memory	4 KB, and supports Flash memory content CRC check	12 KB
Flash memory 16-bit write time	40 µs	53.5 µs
Flash memory sector erase time	6.4 ms	30 ms
Flash memory Mass erase time	8 ms	30 ms
SPI	SPI1/SPI2 support I^2S feature	Not support
Security library(sLib)	Support	N/A
Boot memory used as an extension block of main Flash	Support	N/A
User System Data area	256 Bytes	16 Bytes
ADC	2 Msps (max. ADCCLK = 28 MHz)	1 Msps (max. ADCCLK = 14 MHz)
Core voltage	1.2 V, lower operating current	1.8 V
ESD parameters	HBM: 6 kV, CDM: 1000 V	HBM: 2 kV, CDM: 500 V
Run mode	7.5 mA@48 MHz	22.0 mA@48 MHz

	AT32F421	SXX32F030
Power consumption at Sleep mode	5.7 mA@48 MHz	14.0 mA@48 MHz
Power consumption at Deepsleep mode	210 uA	7.9 uA
Power consumption at Standby mode	3.6 uA	4.8 uA

2 Hardware migration

The migration from SXX32F030 to AT32F421 series is very simple as they are pin-to-pin compatible basically, with only a few pins different from SXX32F030CC, as shown in the table below.

Table 2. Hardware pinout compatible

AT32F421		SXX32F030CC	
QFP48	Pinout	QFP48	Pinout
35	PF6	35	V_{SS}
36	PF7	36	V_{DD}

3 Software migration

3.1 Peripheral comparison

There are some differences between AT32F421 and SXX32F030 in terms of peripherals, some of which are new designs for AT32F421 series. Therefore, it is necessary to modify these peripherals or use a new peripheral driver for brand-new design during the application-level program development.

Table 3. Peripheral compatibility analysis

Peripheral	AT32F421	SXX32F030	Compatibility		
			Features	Pinout	Firmware driver
SPI	Y+	Y	SXX32F030: Two FIFOs, 4 to 16-bit data are available. AT32F421: SPI supports I2S function and real-time synchronization between I2S WS line and Data, and AT32F421 SPI baud rate supports up to 50 MHz	Identical	Partial compatibility
WWDT	Y	Y +	Same features	N/A	Full compatibility
WDT	Y	Y +	Added window mode	N/A	Partial compatibility
DEBUG	Y	Y	Same features	N/A	Compatibility
CRC	Y	Y +	Added reverse function and initial CRC value	N/A	Partial compatibility
EXINT	Y	Y +	Some peripherals can generate events in Stop mode	Identical	Partial compatibility
DMA	Y	Y	1 DMA controller with 5 channels	N/A	Partial compatibility
TMR	Y	Y +	Enhancement	Identical	Partial compatibility
PWC	Y	Y +	V_{DDA} can be greater than V_{DD}, 1.8 V mode core	Identical for same feature	Partial compatibility
CRM	Y ++	Y	Enhanced max frequency, AHB, APB and CLKOUT	Identical	Partial compatibility
USART	Y	Y +	Undependent clock source selection, time-out features, Wake up from Stop mode	Identical	Partial compatibility
I^2C	Y	Y	SXX32F030: Communication events managed by hardware, FM+, Wake up from Stop mode, digital filter AT32F421:	Identical	Partial compatibility

Peripheral	AT32F421	SXX32F030	Compatibility		
			Features	Pinout	Firmware driver
			Supports 1 MHz rate		
ADC	Y	Y +	Same analog, but with new digital interface	Identical	Partial compatibility
RTC	Y ++	Y	Backup registers	Identical	Compatibility
FLASH	Y ++	Y	Option bytes extended to 256 bytes, security library function, system memory used as an extended block of main Flash, and supports access by bytes, half-word and word.	N/A	Partial compatibility
GPIO	Y	Y	-	Identical	Partial compatibility
CMP	Y	N/A	-	N/A	N/A
SCFG	Y	Y	-	N/A	Partial compatibility

3.2 Memory mapping

For performance optimization, AT32F421 has been further adjusted in its architecture. In terms of peripheral addresses and bus matrix distribution, there are some differences in AT32F421 versus SXX32F030, shown as follows.

Table 4. Memory map differences

Peripheral	SXX32F030		AT32F421		Conclusion
	Bus	Base address	Bus	Base address	
CRC	AHB1	0x40023000	AHB	0x40023000	Identical
FLASH		0x40022000		0x40022000	Identical
CRM		0x40021000		0x40021000	Identical
DMA		0x40020000		0x40020000	Identical
GPIOF	AHB2	0x48001400		0x48001400	Identical
GPIOC		0x48000800		0x48000800	Identical
GPIOB		0x48000400		0x48000400	Identical
GPIOA		0x48000000		0x48000000	Identical
DEBUG	APB	0x40015800	CPU core	0xE00420000	Different
TMR17		0x40014800	APB2	0x40014800	Identical
TMR16		0x40014400		0x40014400	Identical
TMR15		0x40014000		0x40014000	Identical
USART1		0x40013800		0x40013800	Identical
SPI1		0x40013000		0x40013000	Identical
TMR1		0x40012C00		0x40012C00	Identical
ADC		0x40012400		0x40012400	Identical
USART6		0x40011400		N/A	Different
EXINT		0x40010400		0x40010400	Identical
SCFG		0x40010000		0x40010000	Identical

Peripheral	SXX32F030		AT32F421		Conclusion
	Bus	Base address	Bus	Base address	
CMP		N/A		0x40010000	Identical
PWC		0x40007000		0x40007000	Identical
I^2C2		0x40005800		0x40005800	Identical
I^2C1		0x40005400		0x40005400	Identical
USART5		0x40005000		N/A	Different
USART4		0x40004C00		N/A	Different
USART3		0x40004800		N/A	Different
USART2		0x40004400		0x40004400	Identical
SPI2		0x40003800	APB1	0x40003800	Identical
WDT		0x40003000		0x40003000	Identical
WWDT		0x40002C00		0x40002C00	Identical
RTC		0x40002800		0x40002800	Identical
TMR14		0x40002000		0x40002000	Identical
TMR7		0x40001400		N/A	Different
TMR6		0x40001000		0x40001000	Identical
TMR3		0x40000400		0x40000400	Identical

3.3 Functional differences

This section describes the peripherals between AT32F421 and SXX32F030.

3.3.1 CRM

- The differences related to CRM (Clock and reset management) in the AT32F421 series and SXX32F030 series are presented in the table below.

Table 5. CRM differences

RCC	AT32F421	SXX32F030
HICK	48 MHz RC frequency divided by 6, 48 MHz RC	8 MHz RC
HEXT	4-25 MHz	4-32 MHz
HICK14	N/A	For ADC
CLKOUT	ADCCLK, SYSCLK, LICK, LEXT, HICK, HEXT, PLL/2, PLL/4	HICK14, SYSCLK, HICK, HEXT, PLL/2, PLL, LEXT, LICK, HICK48

3.3.2 CRM PLL

- For the AT32F421, in the system clock configuration process, it is necessary to configure the PLL_FREF parameters (CRM_PLL[26:24]) in the reference configuration table according to the PLL clock source used before programming and enabling CRM PLL.

3.3.3 DMA interface

- The differences related to DMA in AT32F421 series versus SXX32F030 are presented in the table below.

Table 6. DMA differences

Peripheral	DMA request	AT32F421	SXX32F030	Conclusion
TMR17	TMR17_UP TMR17_CH1	DMA_Channel1/DMA_Channel2 DMA_Channel1/DMA_Channel2	DMA_Channel1/DMA_Channel2 DMA_Channel1/DMA_Channel2	Identical
TMR16	TMR16_UP TMR16_CH1	DMA_Channel3/DMA_Channel4 DMA_Channel3/DMA_Channel4	DMA_Channel3/DMA_Channel4 DMA_Channel3/DMA_Channel4	Identical
TMR15	TMR15_UP TMR15_CH1 TMR15_TRIG TMR15_COM	DMA_Channel5 DMA_Channel5 DMA_Channel5 DMA_Channel5	DMA_Channel5 DMA_Channel5 DMA_Channel5 DMA_Channel5	Identical
USART1	USART1_Rx USART1_Tx	DMA_Channel3/DMA_Channel5 DMA_Channel2/DMA_Channel4	DMA_Channel3/DMA_Channel5 DMA_Channel2/DMA_Channel4	Identical
SPI1	SPI1_Rx SPI1_Tx	DMA_Channel2 DMA_Channel3	DMA_Channel2 DMA_Channel3	Identical
TMR1	TMR1_UP TMR1_CH1 TMR1_CH2 TMR1_CH3 TMR1_CH4 TMR1_TRIG TMR1_COM	DMA_Channel5 DMA_Channel2 DMA_Channel3 DMA_Channel5 DMA_Channel4 DMA_Channel4 DMA_Channel4	DMA_Channel5 DMA_Channel2 DMA_Channel3 DMA_Channel5 DMA_Channel4 DMA_Channel4 DMA_Channel4	Identical
ADC	ADC	DMA_Channel1 DMA_Channel2	DMA_Channel1 DMA_Channel2	Identical
I^2C2	I2C2_Rx I2C2_Tx	DMA_Channel5 DMA_Channel4	DMA_Channel5 DMA_Channel4	Identical
I^2C1	I2C1_Rx I2C1_Tx	DMA_Channel3 DMA_Channel2	DMA_Channel3 DMA_Channel2	Identical
USART2	USART2_Rx USART2_Tx	DMA_Channel5 DMA_Channel4	DMA_Channel5 DMA_Channel4	Identical
SPI2	SPI2_Rx SPI2_Tx	DMA_Channel4 DMA_Channel5	DMA_Channel4 DMA_Channel5	Identical
TMR6	TIM6_UP	DMA_Channel3	DMA_Channel3	Identical
TMR3	TMR3_UP TMR3_CH1 TMR3_TRIG TMR3_CH3 TMR3_CH4	DMA_Channel3 DMA_Channel4 DMA_Channel4 DMA_Channel2 DMA_Channel3	DMA_Channel3 DMA_Channel4 DMA_Channel4 DMA_Channel2 DMA_Channel3	Identical
USART3	USART3_Rx USART3_Tx	N/A	DMA_Channel3 DMA_Channel2	Different

3.3.4 Interrupt vectors

- There are slight differences related to interrupt vectors in AT32F421 series versus SXX32F030 series, as presented in the table below.

Table 7. Interrupt vector differences

Position	AT32F421	SXX32F030	Conclusion
0	WWDT	WWDG	Identical
1	PVM	Reserved	Identical
2	ERTC	RTC	Identical
3	FLASH	FLASH	Identical
4	CRM	RCC	Identical
5	EXINT0_1	EXTI0_1	Identical
6	EXINT2_3	EXTI2_3	Identical
7	EXINT4_15	EXTI4_15	Identical
8	Reserved	Reserved	Identical
9	DMA_CH1	DMA_CH1	Identical
10	DMA_CH2_CH3	DMA_CH2_CH3	Identical
11	DMA_CH4_CH5	DMA_CH4_CH5	Identical
12	ADC_CMP	ADC	Identical
13	TMR1_BRK TMR1_UP TMR1_TRG TMR1_COM	TIM1_BRK_UP_TRG_COM	Identical
14	TMR1_CH	TIM1_CC	Identical
15	Reserved	Reserved	Identical
16	TMR3	TIM3	Identical
17	TMR6	TIM6	Identical
18	Reserved	Reserved	Identical
19	TMR14	TIM14	Identical
20	TMR15	TIM15	Identical
21	TMR16	TIM16	Identical
22	TMR17	TIM17	Identical
23	I2C1_EVT	I2C1	Different
24	I2C2_EVT	I2C2	Different
25	SPI1	SPI1	Identical
26	SPI2	SPI2	Identical
27	USART1	USART1	Identical
28	USART2	USART2	Identical
29	Reserved	USART3_4_5_6	Different
30	Reserved	Reserved	Identical
31	Reserved	Reserved	Identical
32	I2C1_ERR	Reserved	Different
33	Reserved	Reserved	Identical
34	I2C2_ERR	Reserved	Different

3.3.5 GPIO interface

- The main difference related to GPIO between AT32F421 and SXX32F030 is that the AT32F421 output mode does not support internal pull-up and pull-down.

Table 8. GPIO differences

GPIO	AT32F421	SXX32F030
Input mode	Floating PU PD	Floating PU PD
Output mode	PP	PP PP+PU PP+PD
	OD	OD OD+PU OD+PD
Alternate function	PP	PP PP+PU PP+PD
	OD	OD OD+PU OD+PD
20 mA sinking strength	Not support	Support

3.3.6 ADC interface

- The differences related to ADC in AT32F421 series versus SXX32F030 series are presented in the table below.

Table 9. ADC differences

ADC	AT32F421		SXX32F030
Number of channels	15 channels + 3 internal channels		16 channels + 2 internal channels
Conversion modes	Sequence/Repetition/Partition/Automatic preempted group conversion		Single/Continuous/Discontinuous/Scan
Resolution	12-bit		12-bit
Max sampling frequency	2 MSPS		1 MSPS
External trigger	Ordinary group TMR1 CH1 TMR1 CH2 TMR1 CH3 TMR3 TRGOUT TMR15 CH1 EXINT line11 SWSTR	Preempted group TMR1 TRGOUT TMR1 CH4 TMR3 CH4 TMR15 TRGOUT EXINT line15 SWSTR	External events TIM1_TRGO TIM1_CC4 TIM3_TRGO TIM15_TRGO

3.3.7 SPI interface

- AT32F421 removes the following SPI features versus SXX32F030:
  1. NSS pulse mode configuration and TI mode configuration
  2. Programmable data frame size
  3. Tx/Rx FIFO buffers

  AT32F421 has additional features as follows:
  1. SPI can be used as I^2S feature
  2. Support real-time synchronization between I2S WS and Data
  3. SPI baud rate up to 50 MHz

3.3.8 I2C

- There are big differences between the I^2C interfaces of AT32F421 series versus SXX32F030 series. The architecture, features and programming interface are different. Therefore, any code written for the SXX32F030 series using the I^2C needs to be rewritten to run on the AT32F421 series.

3.3.9 USART

- The AT32F421 series embeds a different USART peripheral versus SXX32F030. The architecture, features and programming interface are different. Therefore any code written for the SXX32F030 series using the USART needs to be rewritten to run on the AT32F421 series.

3.3.10 PWC

- AT32F421 cancels PA2 and PC5 as wkup pins versus SXX32F030,
- AT32F421 adds extra low-power mode of interal voltage regulator in Deepsleep mode versus SXX32F030

3.3.11 Security library (sLib)

- Security library (sLib) feature is provided to prevent important IP-Code from being modified or read by end applications so as to enhance security level.

3.3.12 GPIO 5V-tolerant compatibility

- AT32F421 provides more 5V-tolerant input pins compared to SXX32F030, except PC14, PC15, PF0 and PF1 (the input level of these pins should not exceed VDD + 0.3V).
- All other pins are 5V-tolerant.

4 Revision history

Table 10. Document revision history

Date	Revision	Changes
2022.02.25	2.0.0	Initial release
2022.10.18	2.0.1	Added *3.3.10 PWC*
2022.11.2	2.0.2	Updated the description of *3.3.10 PWC*

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